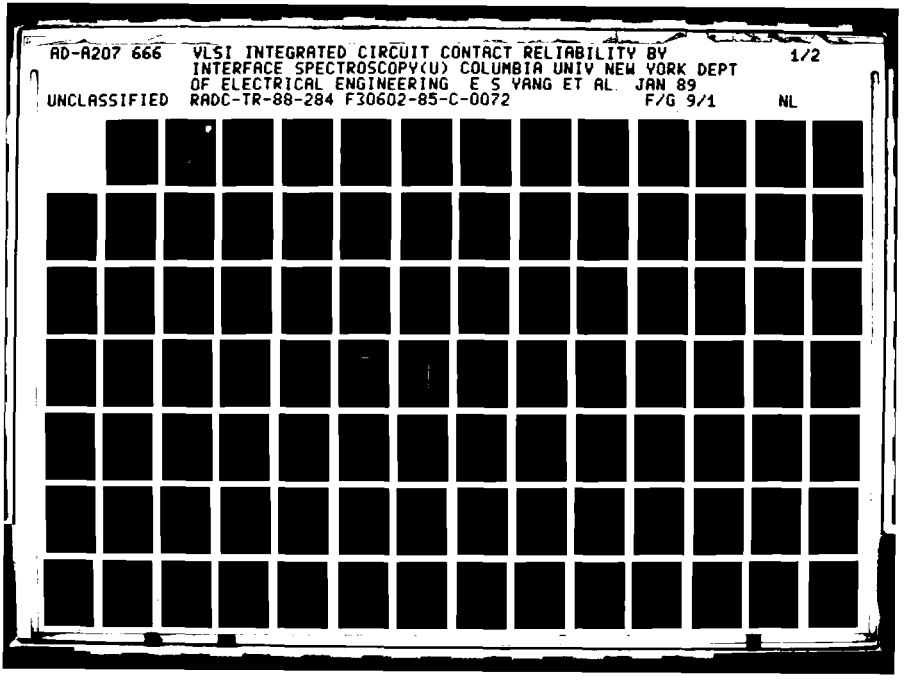
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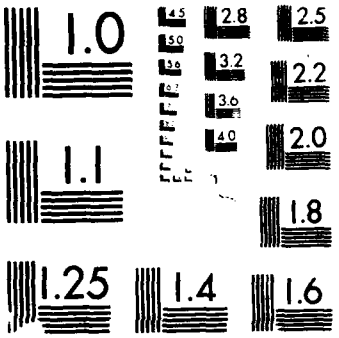
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January 1989

VLSI INTEGRATED CIRCUIT CONTACT RELIABILITY BY INTERFACE SPECTROSCOPY

Columbia University

E. S. Yang and H. Evans

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ROME AIR DEVELOPMENT CENTER
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Metal semiconductor contacts comprise one of the most important interfaces in modern microelectronics. However, the underlying physical mechanisms which lead to their gross electrical characteristics are not well understood. The thrust of our work under AFOSR Contract No. F-30602-85-C-0072 has been to explore the microscopic origins of the energy barrier present at the metal semiconductor interface. We feel that only with such an understanding can the degradation and reliability of ohmic and rectifying contacts be understood and hence better controlled. The work we will report can be divided into three separate, but yet very inter-related, topics. First, we developed and utilized forward bias capacitance techniques for determining the interface state distribution in silicon Schottky diodes. These techniques were applied to as deposited and annealed palladium silicon diodes as well as epitaxial and nonepitaxial nickel silicide structures. Furthermore, they were found to be useful in explaining the effect of a blocking contact on minority carrier concentrations in pn junctions. We then developed a method to vary

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the Schottky barrier height on gallium arsenide in a controllable manner. This was done by using a laser enhanced oxidation technique which resulted in the formation of very thin stoichiometric or gallium rich oxide layers. A deep level transient spectroscopy investigation of these devices resulted in an increased understanding of the effect of the barrier height on DLTS signals. These devices served as the test vehicle for the third major study being reported. The reverse biased capacitance spectra of GaAs diodes yields data not easily interpreted in terms of the barrier height and doping density. We suggest an explanation for this discrepancy which is related to the pinning of the Fermi level seen in GaAs and not in silicon. This work is still in progress and promises some exciting results.

EVALUATION

This contract was successful in applying the forward bias capacitance technique to Schottky barrier diodes. The contractor proposed this approach. Diligent and innovative work on the part of the investigators produced information for all or part of five papers published in the open literature. The work was performed as scheduled, and has provided insight relative to instability problems seen in Schottky devices.

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Chapter 1 - Forward Bias Capacitance Spectroscopy

Metal semiconductor contacts play a prominent role in integrated circuit technology. Indeed, it is widely recognized that they impose critical limitations on the speed and reliability of VLSI circuits.[1] Despite their importance, many fundamental questions concerning the formation and behavior of these interfaces remain unanswered. We have addressed these problems using new techniques developed in our laboratory to study the physics of contact formation. In this chapter we will briefly describe metal semiconductor interface formation and previous techniques used to study the contacts. Our analysis methods, their limitations, theoretical models and typical experimental results will then be discussed.

Carrier transport across a metal semiconductor interface is governed by the height of the energy barrier at the junction. It is not yet understood, however, what determines the barrier height for a given metal semiconductor system. The first model put forward to explain the barrier height was that of Schottky in 1937.[2] In Schottky's model there is no interface region nor any interface states, just the metal of work function ϕ_m and the semiconductor with electron affinity x_s and work function $\phi_s < \phi_m$. When the semiconductor and metal are joined, alignment of the Fermi level and vacuum level at the interface leads to a band bending in the semiconductor and a barrier height (looking from the metal towards the semiconductor) given by

$$\Phi_{Bn} = (\phi_m - X_s)$$

However, practical metal semiconductor contacts do not appear to obey the above guideline. As shown in Figure 1 the experimental results of barrier heights for metal n-type silicon contacts lead to a much less sensitive function of Φ_m than given in Eq.(1). An attempt to explain this insensitivity of barrier height to the metal work function was given by Bardeen in 1947.[3] Bardeen proposed the existence of surface states intrinsic to the semiconductor which are unaffected by metal deposition. These surface states are responsible for the formation of a barrier at the free semiconductor surface even in the absence of metal. When a metal is brought into contact with the semiconductor, equilibrium is reached by the semiconductor exchanging charge with the metal. If the density of surface states at the semiconductor surface is very large, the charge exchange takes place from the surface states to the metal and the space charge and energy barrier in the semiconductor remain unaffected. In the Bardeen limit, therefore, the barrier height is independent of the metal and determined solely by the semiconductor. The Fermi level is pinned by the semiconductor surface states. Again Figure 1 shows that this is not completely correct.

Cowley and Sze[4] attempted to combine the theories of Schottky and Bardeen into a more generalized theory for the Schottky barrier height. They proposed an interfacial layer a few angstroms thick essentially transparent to electrons and semiconductor surface states unaffected by metal deposition. Using empirical data they determine constants c_2 and c_3 such that a general expression for the barrier height is obtained

$$\Phi_{Bn} = C_2 \Phi_m + C_3$$

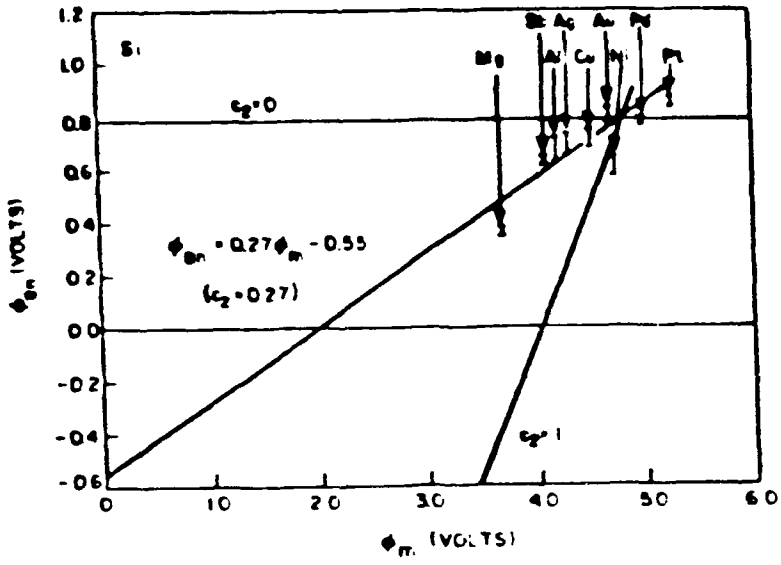


Figure 1. Experimental results of barrier heights for metal n-type silicon contacts.

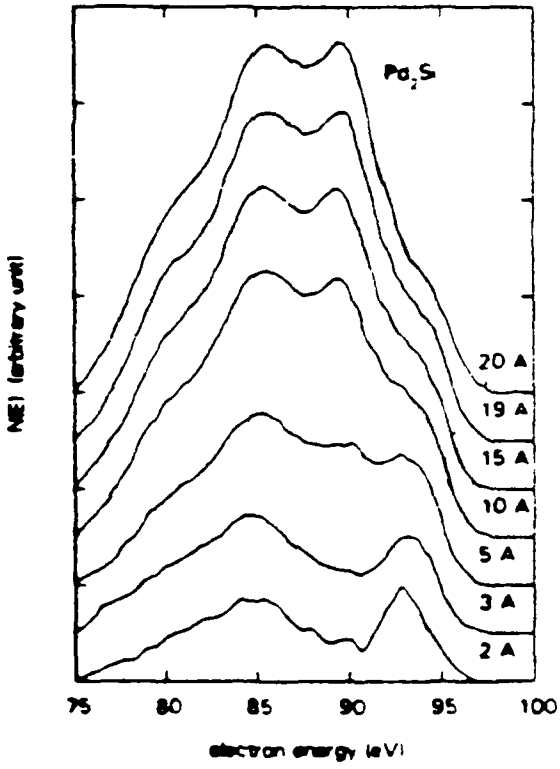


Figure 2. AES study for palladium deposition on silicon. Note the difference in the spectra for the 2 A coverage where interface effects dominate, and the 20 A coverage where bulk silicide effects dominate.

Their result for silicon is shown in Figure 1.

Both the Cowley and Sze and Bardeen's model assume the semiconductor surface is unaffected by the metal deposition process. However, for the clean GaAs (110) surface there are no surface states in the gap. Yet GaAs barrier heights show only a weak dependence on the metal work function. This leads us to believe that other interface states are responsible for pinning the Fermi level. Evidence of metal induced surface states is rather extensive. It is now believed that intrinsic surface states are unimportant and the barrier height is due to defects formed near the interface by deposition of the metals. Spicer et. al. have proposed a model of barrier formation on III-V compound semiconductors based on the creation of vacancies and antisites in the semiconductor.[5] Donor and acceptor type interface states arise in the bandgap of the semiconductor and are responsible for pinning the Fermi level. This pinning of the surface Fermi level can explain the fact that for most III-V compounds, the barrier height is essentially independent of the metal work function. The key consideration is that a more precise knowledge of the microscopic structure of the metal-semiconductor interface and a measurement of the interface states is necessary in order to determine what pins the Fermi level and gives the barrier height in a Schottky barrier.

Various techniques have been proposed to solve this problem. Energetic beam spectroscopies, such as Auger Electron Spectroscopy (AES) and Ultraviolet Photoemission Spectroscopy (UPS), have shed considerable light on the processes which occur during interface formation. In these

spectroscopies an incident energy, an electron in the case of AES, a photon of UV light in the case of UPS, initiates transitions resulting in the emission of an electron from the sample. Electrons within an "escape depth" (10 A) of the surface are released without having undergone any scattering or energy loss. The distribution of energies of the emitted electrons provides a signature of the energy states available for electron occupancy within an escape depth of the surface. In the search for interface states at the silicide/silicon interface, data from energetic beam spectroscopies suggest several electronic states localized at these interfaces. For example, the results of an AES study for palladium deposited on silicon are shown in Figure 2.[6] In this work the shape of the AES spectra was studied as a function of Pd coverage at room temperature. The Auger line investigated was a certain Si transition (LVV). Since many techniques have clearly established that the first 10-15 A of Pd deposited at room temperature react to form a silicide like compound, contributions to the data comes from silicon in the elemental silicon substrate, the stoichiometric Pd_2Si overlayer, and the localized region at the interface. At 20 A of Pd_2Si, the substrate no longer contributes due to the short electron escape distance. In the figure, the silicon substrate contribution has been subtracted out. At high coverage the spectrum is essentially that for the Si in the bulk Pd_2Si compound, while at low coverage it has a very strong contribution from the Si atoms in the interface layer. This interface portion has a distinctly different spectral shape from that of Pd_2Si or pure Si. Energy states exist here not found in the other two regions. A possible conclusion is that this difference represents chemical bonds and environment unique to the

interface atoms. This is understandable since the chemical environment of the Si atoms within the first two monolayers outside the bulk silicon is Si rich and distinctly different than that in the silicide. Additionally, UPS data for initial Pt coverages on Si reveals the same result;[47] energy states unique to the interface.

The observation of the existence of true interface states by these surface spectroscopies is an important one. Unfortunately these measurements are not sufficiently accurate to determine their energy level in the bandgap where resolution on the order of .1 eV is needed. In addition, they are not sensitive enough to detect an amount of interface states 10^{12} cm^{-2} which is capable of pinning the Fermi level. This density represents less then 1 interface state for every 1000 surface atoms; AES has a usual sensitivity of only 1 part in 100. Furthermore, the interface can only be probed, a signal from the interfacial region can only be received, when the metal or silicide coverage is less than an electron escape depth (10-20 A). This makes it impossible to get information from these techniques on the interface state distribution in completed Schottky barriers with thick metal overlayers. If the Schottky barrier is made and ion sputtering is used to remove the metal so that surface spectroscopes can be applied to the interface states, it is not clear what effect this procedure will have on the state distribution. Moreover, even when probing an interface with only monolayers of coverage, the signal will consist of contributions from the substrate and the covered layer, in addition to that from the interface. Extracting information from the latter becomes uncertain. Other types of spectroscopies are needed to get the desired information.

Two other techniques that are actively being employed in this area, inverse photoemission spectroscopy[58] and scanning tunneling microscopy,[59] deserve particular mention. In inverse photoemission spectroscopy a pulsed laser excites the semiconductor surface and ultraviolet photoemission measurements are used to determine the energy of the excited electrons. Recent results on Au-GaAs interfaces indicate a prominent state .5 eV above the valence band maximum. In scanning tunneling microscopy the tunneling current between a probe tip riding a few angstroms above the semiconductor surface and the semiconductor is used to map the surface. By scanning the voltage or currents involved and superimposing a small ac signal, it is possible to observe electronic states present at the semiconductor surface. This technique has been applied to the 7 × 7 reconstructed Si (111) surface and states indigenous to this surface have been observed. Unfortunately both of these techniques cannot be applied to complete Schottky barriers with thick metal overlayers.

We have developed an electrical spectroscopy for determining interface state distribution based on capacitance measurement. Measurement of device capacitance is a major, nondestructive electrical technique for obtaining information on impurity concentrations and trap levels in semiconductor devices. When trap levels charge and discharge under the influence of an applied signal, capacitive and conductive elements result as in the equivalent device model. Various modifications of this basic principle have arisen (deep level transient spectroscopy, capacitance voltage profiling, photo capacitance, etc,) in order to isolate the effects of traps in different regions of the

semiconductor or at different energy levels. One such modifications as implemented by Nicollian and Geotzberger[10] is routinely used to characterize the oxide-semiconductor interface in metal-oxide-semiconductor (MOS) structures. Basically this technique involves sweeping the Fermi level past the interface state energy level so that the trap state changes occupancy and contributes to the capacitance and conductance of the structure. When one attempts to apply the same theory and procedure to metal-semiconductor (MS) contacts, however, results are much harder to obtain. The major difficulty in applying the MOS technique to the MS structure is that the majority-carrier Fermi level must be swept through the band gap in order to obtain information about interface levels in the gap. This means that the MS structure must be in the forward-biased regime.[11] In the MOS structure the large energy barriers presented by the oxide inhibit current flow from the silicon to the gate. There is essentially no current flow and aside from the conductance due to the interface states, there is negligible real component of the admittance. In the forward-biased Schottky diode, on the other hand, there is a huge conductance due to the thermionic emission of carriers from the semiconductor to the metal. This huge real component, Gp, overwhelms the imaginary capacitive component, ωCp, making measurements extremely difficult. Indeed, for low-frequency measurements, values of Gp are commonly 10^2-10^4 times as large as ωCp. Usual methods of separating the two components by simply tuning the phase of a phase sensitive detector without the device in place do not give the required accuracy for full deconvolution.

Two systems have been designed in our laboratory to solve the problems associated with these measurements. In Fig. 3 is shown an apparatus for implementing accurate phase forward bias capacitance measurement. The diode is represented by the small-signal conductance, Gp, in parallel with the small-signal capacitance, Cp. To set the phase and ensure that it is set correctly, a parallel test resistor of reasonably large conductance is placed in the circuit. If the phase is incorrectly set and a test resistor is placed between A and B in parallel with Cp, the measured value of Cp will change. However, if the phase is perfectly set, no pure conductance between A and B will influence the measurement of Cp. To correctly set the phase, measurements of Cp are made at a given bias and small-signal level (5 mV) with and without the test resistor. The phase is tuned until both measurements are equal.

Although relatively straightforward in theory, implementation of this method requires considerable care. First, the internal series resistance of the sources and measuring equipment must be kept small, or shunted, so that the test resistor is indeed placed in parallel with the circuit conductance. However, it must be noted that an attempt to use a source with negligible series resistance failed until an external series resistor was inserted and then shunted. Second, the diode bias must be monitored in some way to ensure that it is operating at the same quiescent point with and without the test resistor. In addition, two characteristics of the lock-in amplifier (LIA) must be taken into consideration. In operating the LIA there is an inherent tradeoff between the output stability and the dynamic range. We find that using the highest dynamic range, and hence the lowest output stability is most

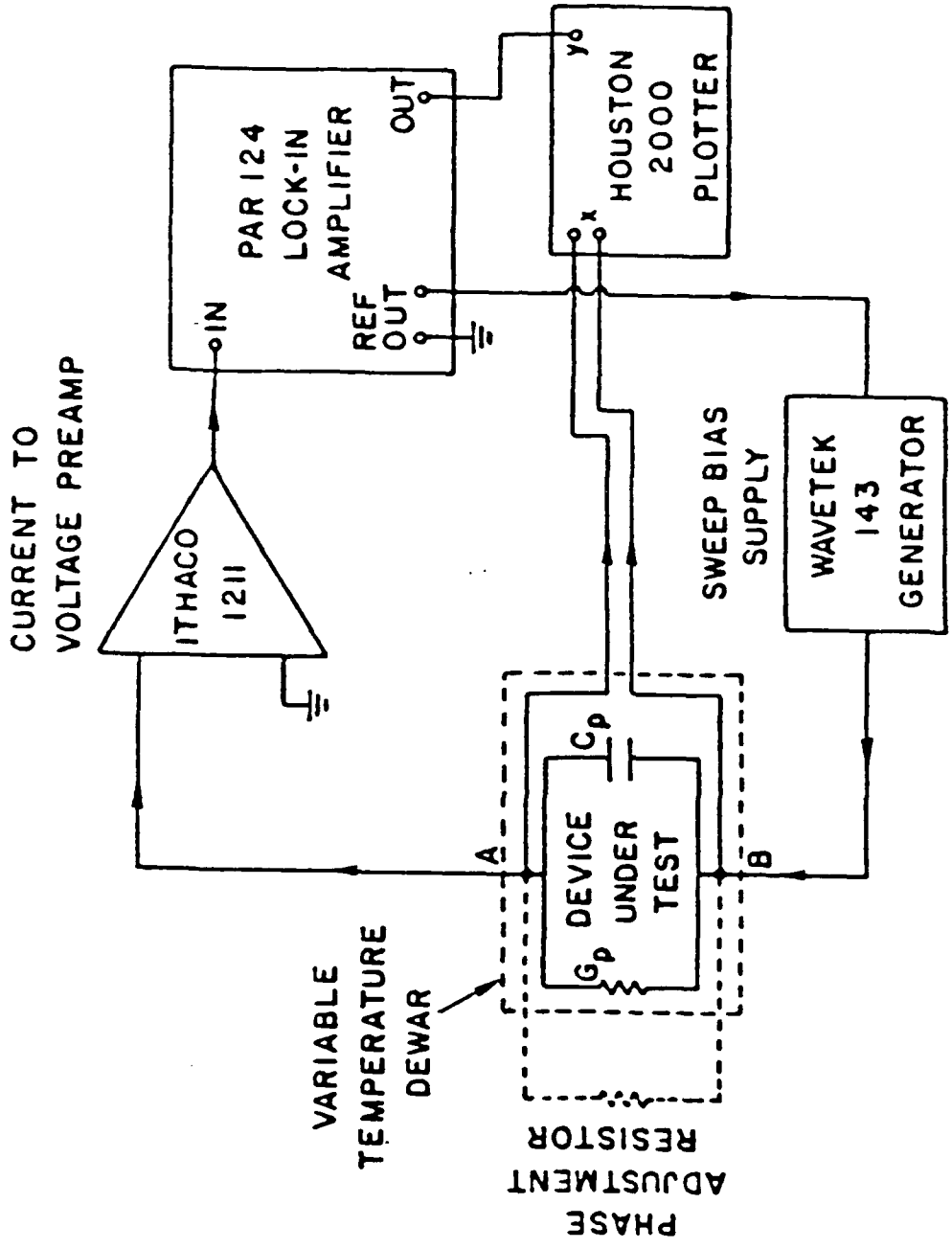


Figure 3. Accurate phase capacitance spectroscopy apparatus.

convenient in this measurement. However, when using the high sensitivity required to determine the capacitance, the conductance can attain a value which causes the LIA to enter a nonlinear regime. The capacitance measurements are then in error and rise as shown in Fig. 4. This problem can be overcome by inserting a resistor in series with the device which keeps the net conductance from rising excessively high. In setting the phase, the test element will be placed in parallel with the device and this series resistor. The device capacitance can then be derived from the measured values using a simple circuit analysis.

An alternate method of measuring the capacitance based on a differential voltage technique eliminates some of the aforementioned problems but is more tedious to apply. The basic concept of the differential voltage capacitance spectroscopy (DVCS) is similar to that of a bridge circuit. Since the main problem arises from the high conductance that is inherently associated with the device, we generate an in-phase signal to cancel out the conductive component of the diode, retaining only the capacitive component to pass through the phase sensitive detector. This way, the overload problem is avoided and the influence of the phase drift is also minimized. As a result the accuracy of the measurement is greatly improved.

A schematic description of the differential voltage capacitance spectroscopy technique is shown in Fig. 5. A small ac reference signal, V_i, derived from the internal oscillator of a PAR 124 lock-in amplifier, is superimposed on a biasing voltage. This combined voltage is applied between point D and the ground. Two currents are generated. One, i_a, passes through

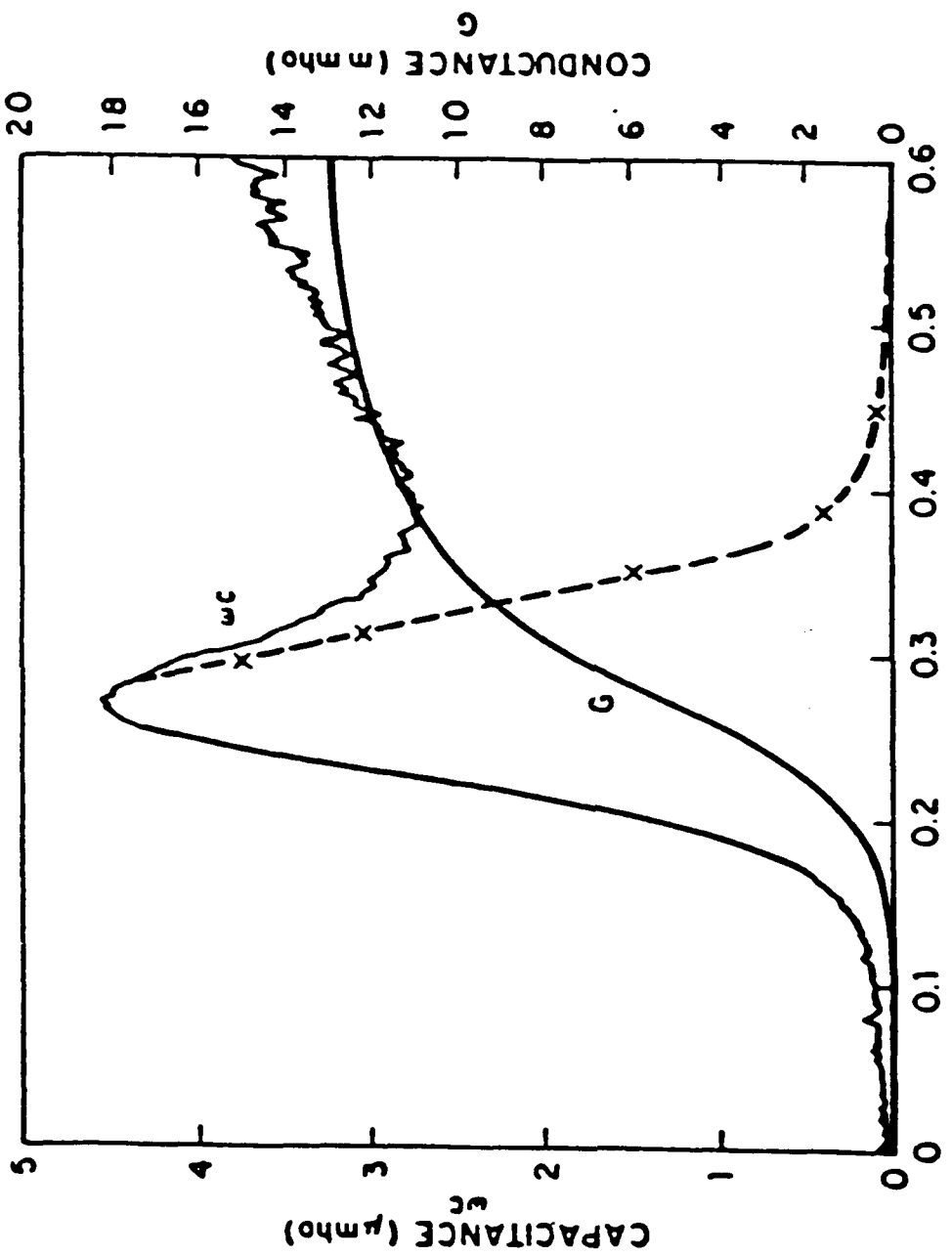


Figure 4. Conductance (G) and capacitance (wC) for a Pd-nSi diode at 104 Hz. Capacitance scale is 4000 times as sensitive as the conductance scale. Note the rising portion of the capacitance above .4V due to the lock-in nonlinearity.

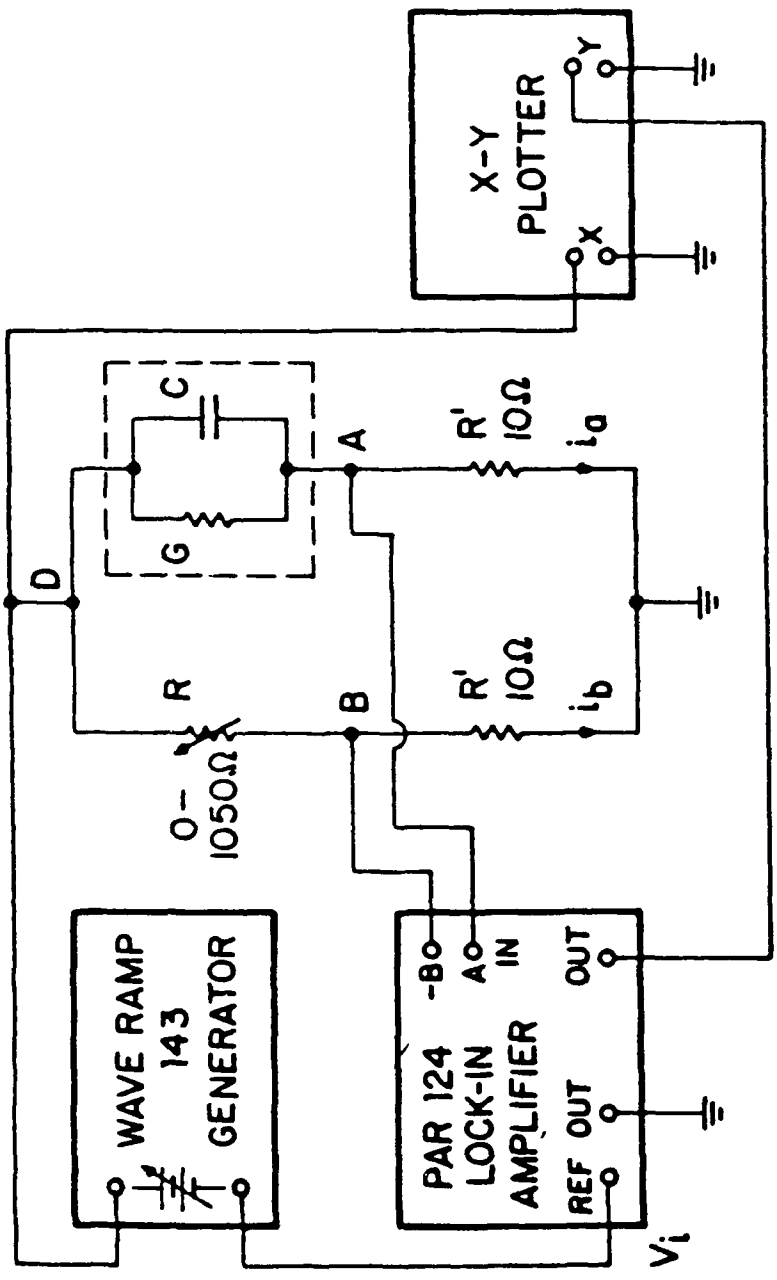


Figure 5. Differential voltage capacitance spectroscopy apparatus.

the diode; the other i_b, through a variable resistor, R. These currents are converted into voltage signals by resistors R', and are then fed into the inputs of the LIA through a differential preamplifier. The output of the differential preamplifier contains only the ac component of V_a - V_b; the dc portion is rejected. If R' is small compared to 1/G and R, the output of the LIA is

$$V_0(\phi) = V_i R' A [(G - 1/R)\cos\phi + \omega C \sin\phi], \tag{3}$$

where A is the voltage gain of the LIA and ϕ the phase setting of the phase sensitive detector. When the phase is set to 90° with a small error $\Delta\phi$, the output becomes

$$V_0 = (90^\circ + \Delta\phi) = V_i R' A [-(G - 1/R)\Delta\phi + \omega C], \tag{4}$$

and the error is

$$\Delta(\omega C) = -(G - 1/R)\Delta\phi. \tag{5}$$

If the conductive component is nulled out, i.e., G - 1/R $\simeq$ 0, the error will be very small even in the presence of a significant $\Delta\phi$.

The measurement procedure is as follows. For each given frequency, the phase of the LIA is first set to 90°. This is accomplished by seeking zero-output when V_b alone is being measured. The resistance R may be chosen to be any value comparable to 1/G of the diode. While keeping the phase-range switch at 90°, the phase vernier is varied until the output of the LIA is zero. Since V_b is in phase with the reference signal, the preceding adjustment ensures that the phase is set to measure only the capacitive component. The next step is to balance the conductive component. For this purpose, we turn the phase-range switch to 0° (without touching the phase vernier) and the

input mode to A-B so that the quantity G - 1/R is examined. The variable resistor R is then adjusted until a zero output is reached. Turning the phase-range switch back to 90°, the output of the LIA is now enitrely due to the capacitance of the diode, i.e.,

$$V_0 = V_i R^2 A\omega C \tag{6}$$

The bias is then scanned manually, the procedure repeated at each voltage and the data collected on the plotter.

Using either of these techniques the device capacitance versus forward bias voltage can be measured at different temperatures and for different small signal frequencies. A series of models have been worked out to explain the data in terms of the interface state distribution. Originally it was thought that the height of the capacitance peak by itself would be reflective of the density of interface states. In that case changes in the capacitance signal alone upon annealing or aging would reveal the changes in interface states occurring at the contact. However, it was soon realized that the capacitance and conductance curves were not independent. For example, a series of experiments in which the device was annealed at different stages in the fabrication cycle showed that increases or decreases in the conductance were followed by similar changes in the capacitance peak especially when large modifications of the conductance occur. It is then difficult to determine whether the changes in the capacitance are due to variations in the interface states or this association with the conductance. Furthermore, changes in the asymptotic value of the conductance, which includes both the series and back contact resistance, upon annealing partially account for the large

conductance changes and hence influence the capacitance data. To eliminate any variation in this parameter an n/n+ epitaxial wafer in which the back contact would be negligibly small was tried. However, it was found, and confirmed with a quick contact resistance study, that with an aluminum ohmic contact and heating less than 400° C for 30 minutes the high voltage conductance was still modified upon annealing. This variation was even seen when an added series resistance of 39 Ω was used to increase the linearity range of the measurement. With a palladium back contact, however, the asymptotic conductance remained constant. Pd/n-n+/Pd and Al/n-n+/Pd devices were fabricated and annealed at 400° C for 30 minutes. The resulting capacitance and conductance curves are shown in Fig. 6. Changes in interface properties are now obvious from the capacitance curves, although numerical interpretation still requires the conductance data.

The first model postulated to explain the data attributed the forward bias capacitance to the current directly charging and discharging the interface states. For this interpretation, palladium silicon diodes were fabricated by thermal evaporation of palladium at 3×10^{-7} Torr onto a chemically etched silicon surface. The silicon substrates were n-type, phosphorous doped, 10 Ω cm, (111) oriented wafers. Chemical cleaning involved a decreasing procedure followed by a CP4 etch. Aluminum was evaporated onto the entire unpolished backside of the wafer to provide a large area ohmic back contact. Current-voltage and forward-biased capacitance measurements were made at various temperatures on the as-deposited sample. The sample was then annealed at 275° C for 30 min in an

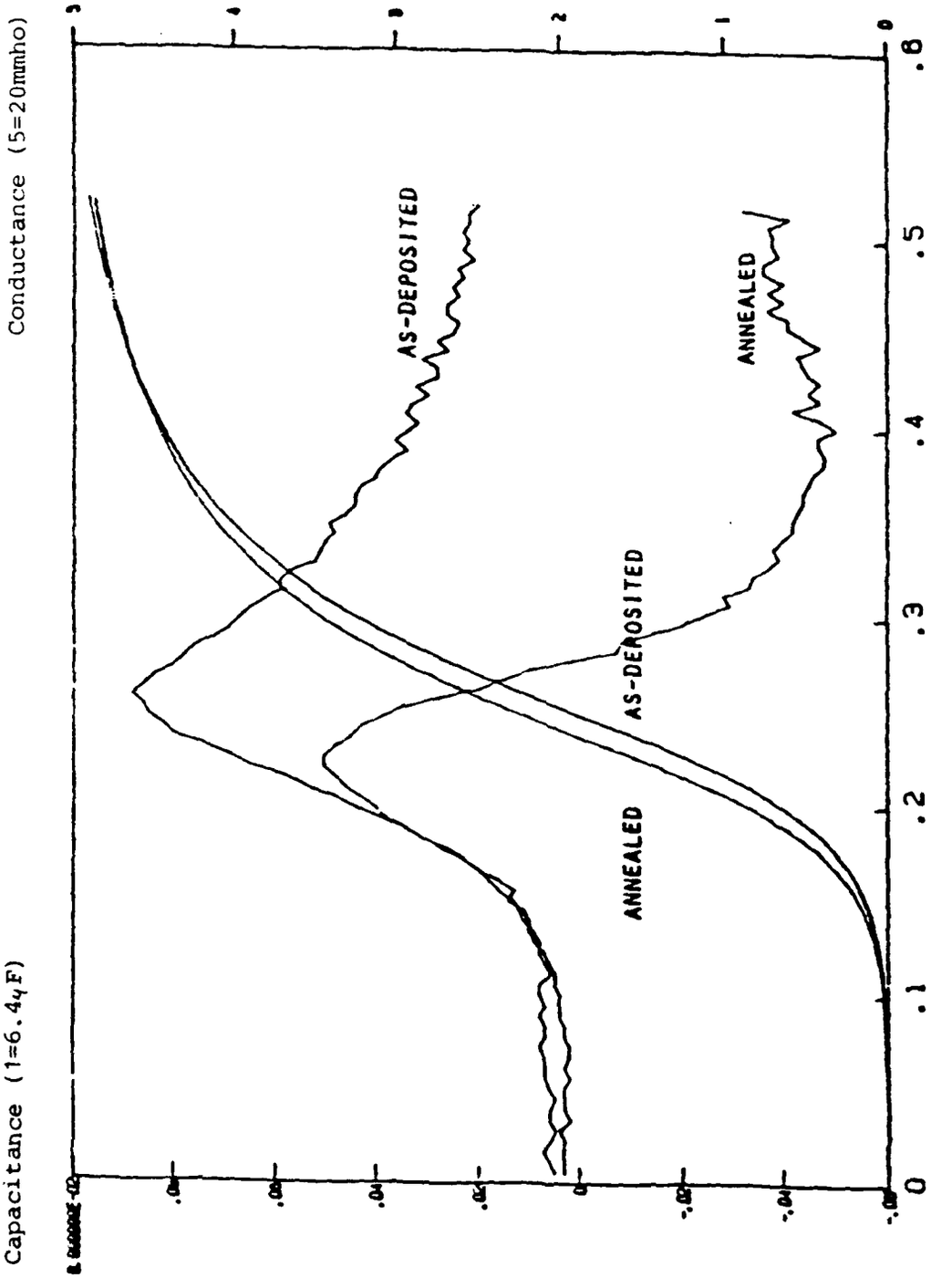


Figure 6. APCS measurements for Pd/n-n+Si/Pd diodes: as-deposited vs. annealed.

argon environment to promote the formation of palladium silicide. After annealing, the diode was subjected to the same measurements at the same temperatures as the as-deposited sample.

Forward-biased capacitance measurements were made at 100 Hz using accurate phase capacitance spectroscopy (APCS). Current-voltage (I-V) measurements were used to determine the barrier height of the diode as well as the resistance of the network in series with the depletion region of the device. This resistance R_S, is assumed to be constant independent of bias but varies with temperature. It consists of the resistance due to the diode neutral region R_{SI} and an external resistance R_{SE} due to the source resistance of the supplies and the diode back contact. It is assumed that the deviation of the dc diode current characteristic from an ideal exponential is due entirely to series resistance so that

$$I = AA^*T^2 e^{-q\Phi_{bn}/kT}\left(e^{q(V_F - IR_s)/kT} - 1\right), \tag{7}$$

where V_F is the voltage applied to the diode, I is the resulting current flow, R_S is the series resistance and A,A*, T,Φ_{bn} are, respectively, the contact area, Richardson's constant, the temperature, and the diode barrier height. Taking two points on the IV curve at a given temperature, the diode series resistance can be determined as

$$R_s = [1/(I_1 - I_2)]kT\ ln\left|(I_2/I_1)e^{-(V_{F2} - V_{F1})/kT}\right|. \tag{8}$$

APCS results at room temperature for both the as-deposited and annealed diode are shown in Fig. 7. I-V characteristics at the same

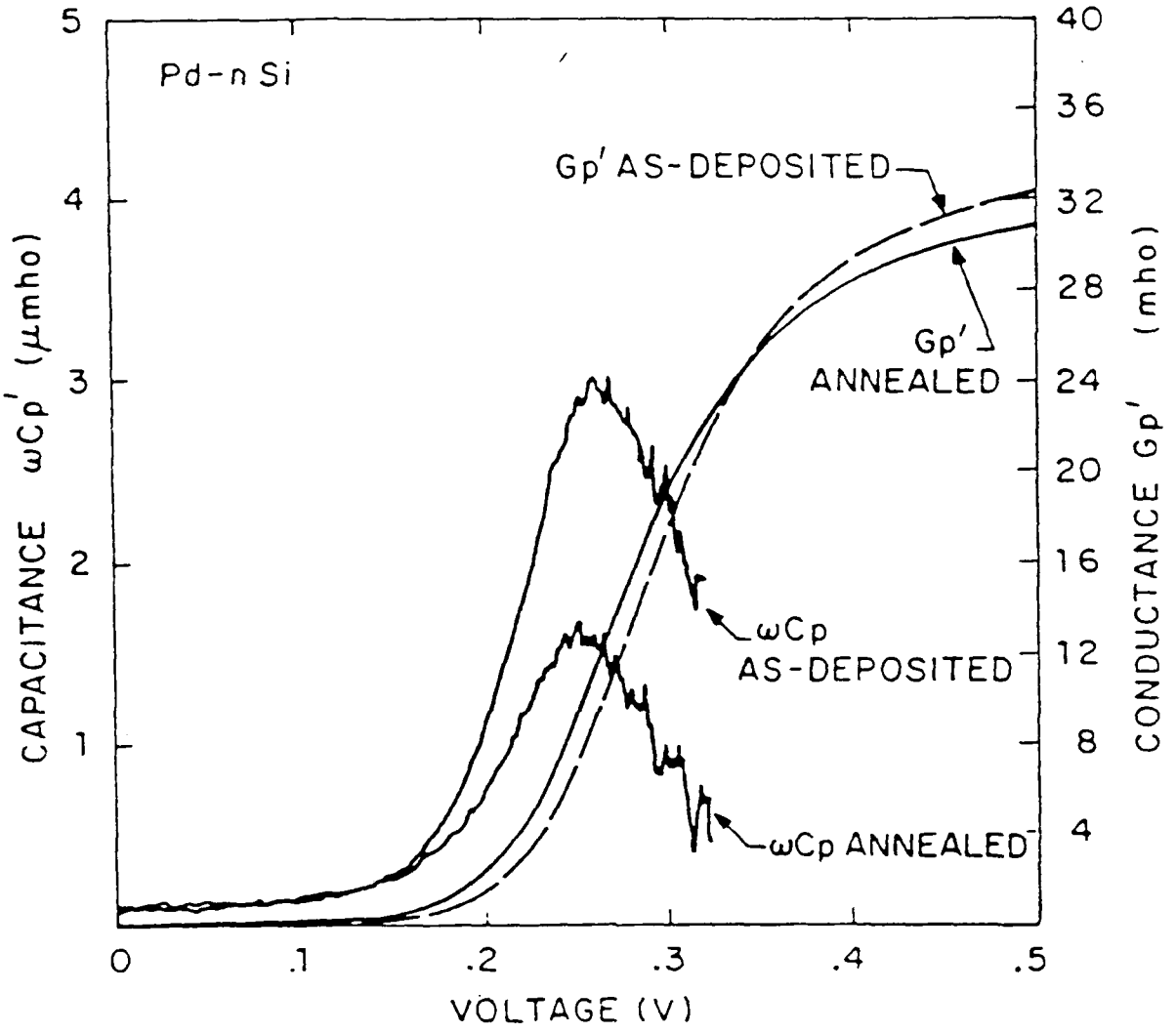


Figure 7. Capacitance (wC) and conductance (G) for the as-deposited and annealed Pd-nSi diode measured at 104 Hz.

temperature are shown in Fig. 8. Ln I vs V_F plots at low applied bias indicate that the room-temperature barrier height changes 8 mV upon annealing from 0.744 to 0.736 eV. In both situations the ideality factor is less than 1.03, revealing good Schottky diodes. Using Eq.(8), the diode series resistance changes with temperature having values of 19, 24, and 26 Ω, for the as-deposited diode and 27, 23, and 33 Ω, for the post annealed diode at 269, 297, and 325 K, respectively.

Before the capacitance due to the interface states can be evaluated in terms of the interface state density, it is necessary to determine this capacitance from the measured circuit parameters. We use the circuit model shown in Fig. 9 where the elements have the following meanings: C_{ss} and G_{ss} are the capacitance and conductance associated with the interface states, C_d is the diode depletion layer capacitance, G_{th} is the conductance due to thermionic emission, and R_s is the series resistance described earlier. The capacitance C_{ss} can be expressed in terms of the measured conductance G_p and capacitance C_p as

$$C_{ss} = \left\{ C_p \left| (1 - G_p R_s)^2 + R_s^2 \omega^2 C_p^2 \right| \right\} - C_d \qquad (9)$$

In our low-frequency measuring regime $R_s w C_p \ll 1 - G_p R_s$ and the right-hand term in the denominator can be neglected. This equation merely represents the effect of the series resistance on the small ac signal. The measured conductance G_p approaches R_s as the thermionic emission conductance G_{th} rises with voltage. More and more of the applied ac signal is then across the series resistor and the effective current through the capacitive

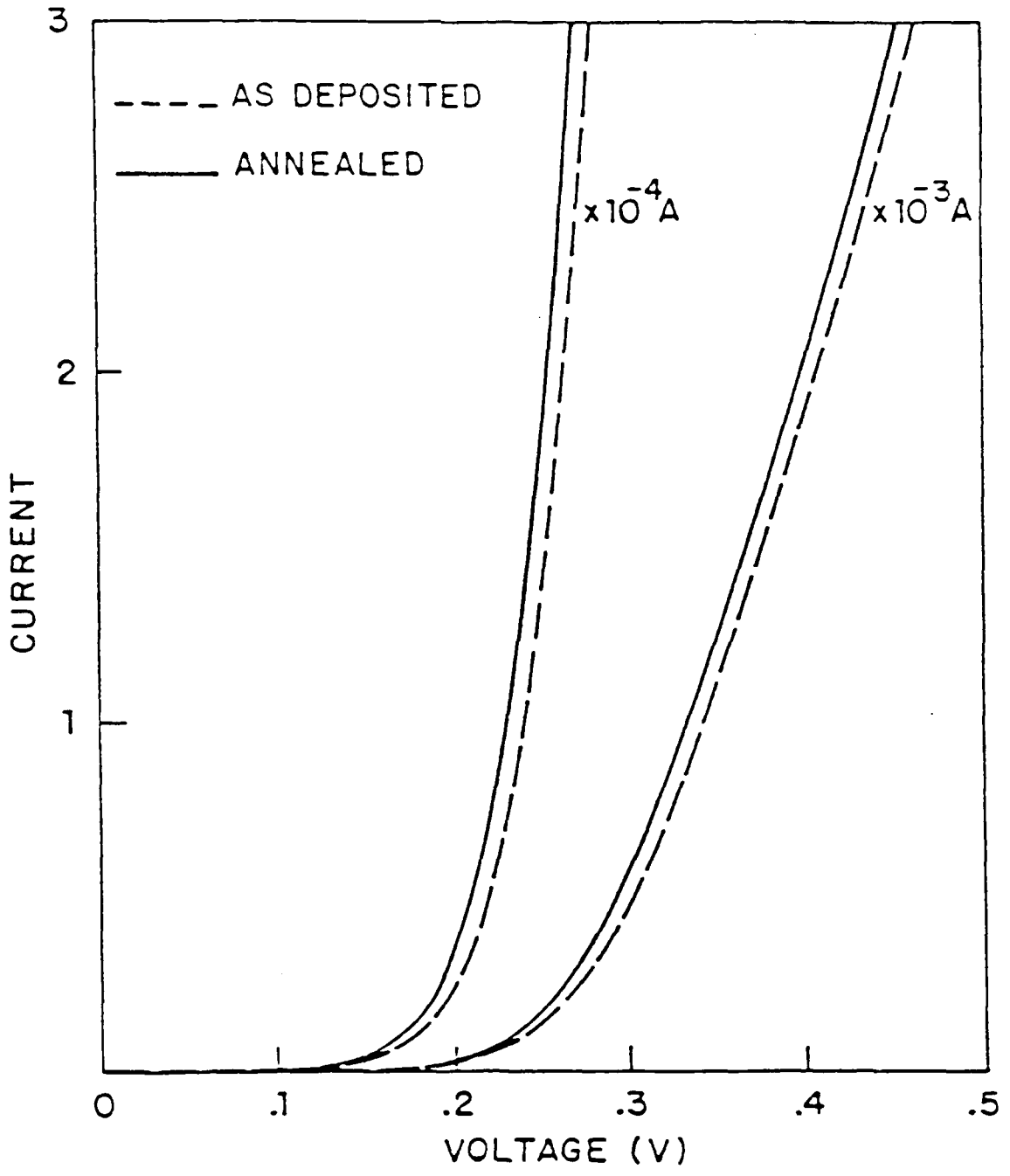


Figure 8. Current voltage measurements at room temperature for the as-deposited and annealed diode. The two sets of curves are for different ordinate scales.

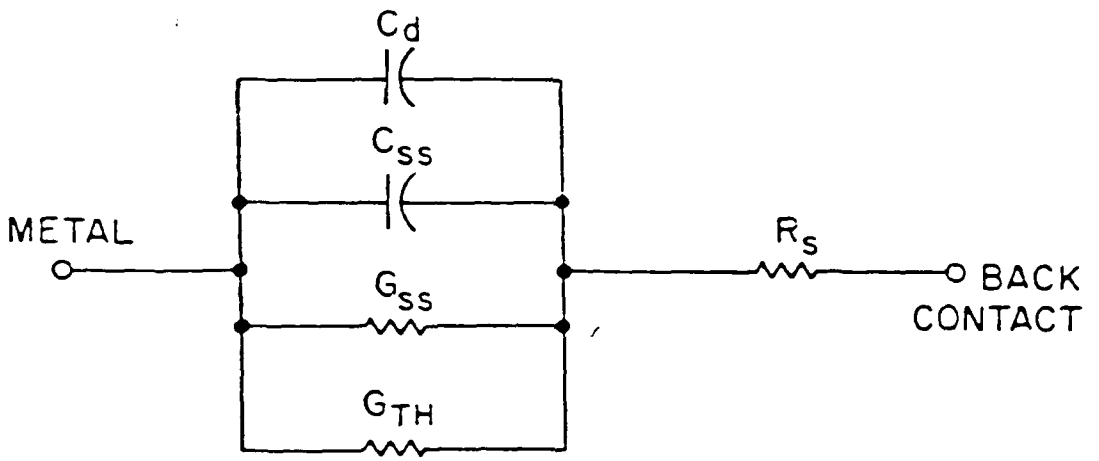


Figure 9. Small signal circuit model of the diode.

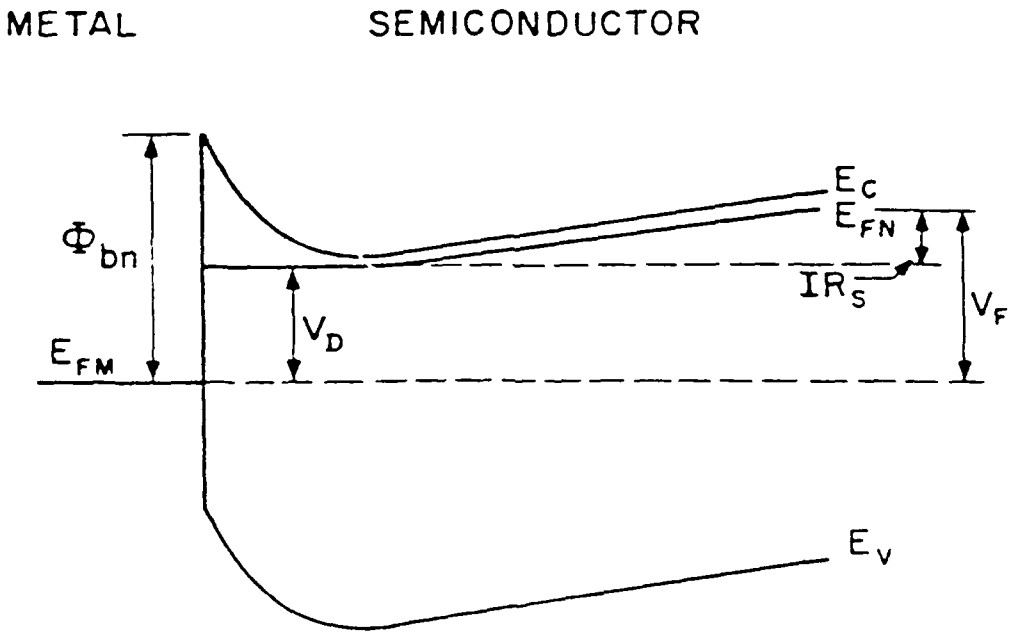


Figure 10. Semiconductor band bending and Fermi level position under forward bias (V_f) in the presence of a series resistance R_s.

elements is reduced accordingly. Equation (9) is needed to account for the changing magnitude of the ac voltage appearing across the active region of the device.

In addition to its effect on the ac signal, the series resistance also influences the position of the Fermi level at the interface. This is shown in Fig. 10 where the band bending and Fermi level split for a given applied bias V_F is shown. The actual dc voltage V_D dropped across the depletion region is reduced from V_F by

$$V_D = V_F - IR_s \tag{10}$$

Assuming the Fermi level is flat throughout the depletion region, the majority carrier density at the surface is given as

$$n_s = N_c e^{-(\Phi_{bn} - V_F + IR_s)/kT} \tag{11}$$

Equation (10) is also needed to determine C_d in Eq.(9), namely,

$$C_d = \left(\frac{q e_s N_d}{2} \right)^{1/2} \left(\Phi_{bn} - V_N - V_D - \frac{kT}{q} \right)^{-1/2}, \tag{12}$$

where N_d and e_s are the doping and permittivity of the wafer, and V_N is the Fermi potential ($kT \ln N_c / N_d$). Using Eqs.(9) and (11), the interface state capacitance C_{ss} for the various cases is shown in Fig. 11. The current-voltage data are taken from the actual I-V curves which, for ease of operation, were considered to be piecewise linear, while the measured conductance G_p is used in Eq.(9).

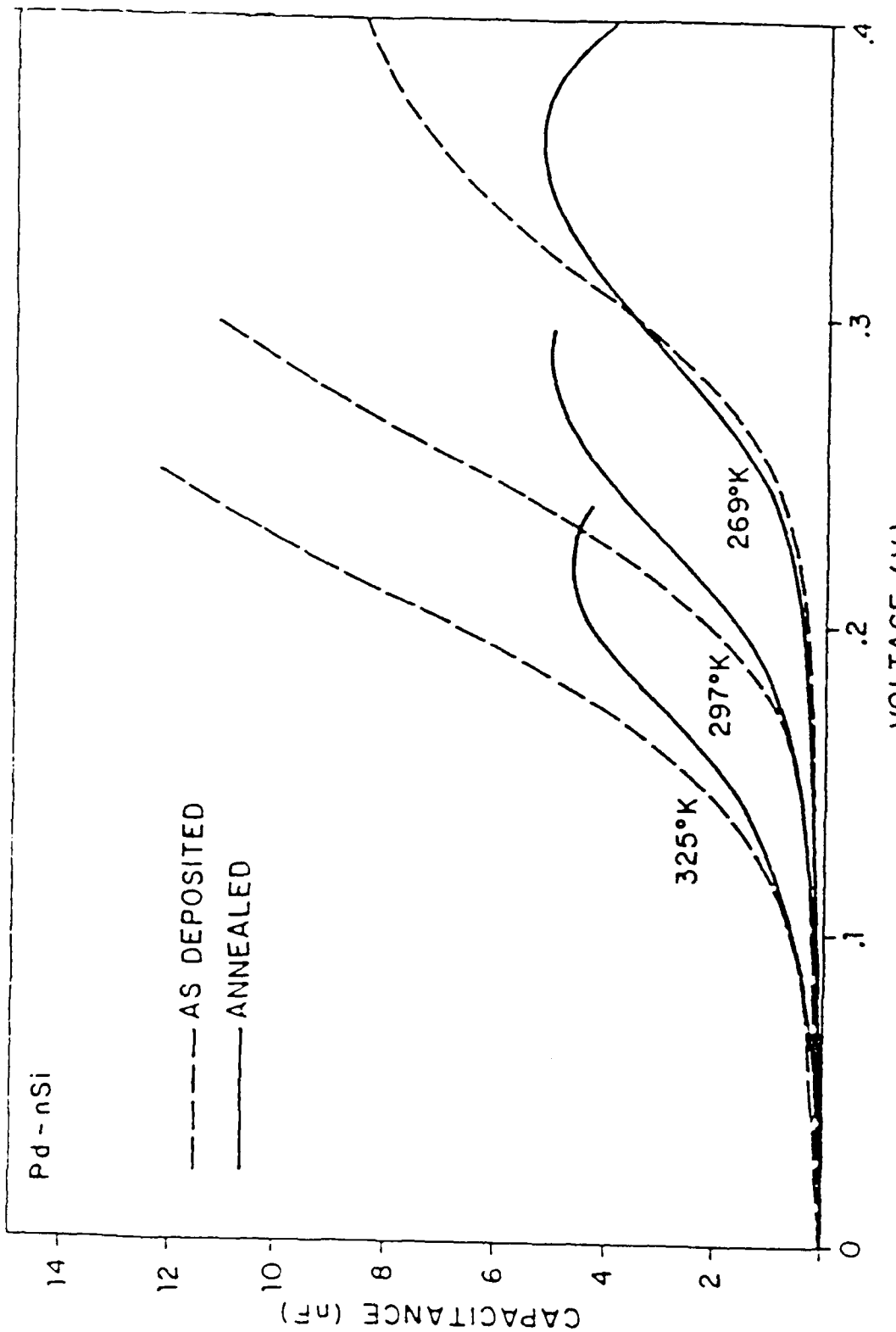


Figure 11. Interface state capacitance (C_{ss}) for the as-deposited and annealed case at 269, 297, and 325 K.

The measured interface state capacitance can be related to the interface state distribution using Shockley-Read-Hall[12] statistics as extended to the interface by Barrett et al.[13] With this model, a given state at energy E_t can exchange charge with the semiconductor conduction and valence bands and the metal according to the rate equations

$$r_a = N_t(1 - F_t)c_n\, n_s, \qquad r_b = N_t\, F_t\, e_n,$$
$$r_c = N_t\, F_t\, c_p\, p_s, \qquad r_d = N_t(1 - F_t)e_p, \qquad (13)$$
$$r_e = N_t(1 - F_t)(1/\tau_c), \qquad r_f = N_t\, F_t(1/\tau_E),$$

where processes *a*, *d*, and *e* refer to capture of an electron from the conduction band, valence band, and the metal, respectively, while processes b, c, and f refer to emission of an electron to the same reserviors. (Communication with the valence band is expressed in terms of capture and emission of holes by the usual convention.) N_T is the level concentration, F_T is the occupancy probability, and c_n (e_n), c_p(e_p) represent the capture (emission) probabilities for electrons and holes. c_n and c_p are usually expressed as a product of a capture cross section and the thermal velocity v_{th} which is temperature dependent according to

$$v_{th}^2 = 3\,kT/m^* \qquad (14)$$

and $1/\tau_c$ and $1/\tau_E$ denote the rate of capture and emission from the metal for a given trap analogous to $c_n n_s$ and e_n. Using the principle of detailed balance under equilibrium conditions, e_n, e_p, and $1/\tau_c$ can be expressed in terms of c_n, c_p, and $1/\tau_E$ and the steady-state occupancy F_T of the level can be found by equating the net current into the trap to zero, viz:

$$F_T = \frac{c_n n_s + c_p p_1 + \left(1/e^{(E_T - E_F)/kT}\right)(1/\tau_E)}{c_n n_s + c_n n_1 + c_p p_s + c_p p_1 + \left(1/e^{(E_T - E_F)/kT}\right)(1/\tau_E) + (1/\tau_E)} , \quad (15)$$

where E_F signifies the metal Fermi level. The charge stored in the trap level under steady-state conditions is then

$$Q_{ss} = q N_t F_T . \quad (16)$$

The low-frequency capacitance due to a single level can be derived using Eq.(16) and the definition of capacitance

$$Q_{ss} = \frac{dQ_{ss}}{dV_D} . \quad (17)$$

The usual assumptions regarding the carrier densities at the surface, n_S and p_S, are made, namely the hole quasi Fermi level is tied to the metal Fermi level and hence p_S is independent of bias, i.e.,

$$\frac{dp_s}{dV_D} = 0 . \quad (18)$$

Using Eq. (11) for n_S gives

$$C_{ss} = \frac{q^2 N_t}{kT}(1 - F_T)F_t \times \frac{c_n n_s}{c_n n_s + c_p p_1 + (1/\tau_E)\left(1/e^{(E_T - E_F)/kT}\right)} \quad (19)$$

The total interface capacitance is then given by a sum over the individual capacitances expressed in Eq. (19) for multiple single levels, or an integral between two energy limits for a band of states.

A computer analysis based on Eq. (19) was used to determine the interface state capacitance resulting from various energy-level distributions and trap parameter sets. The voltage dependence of the measured capacitance requires capture from the conduction band to dominate over the other capture

processes. In addition, the observed temperature shifts indicate capture and emission to be between different charge reservoirs. For all the parameter sets attempted, states closer to the conduction band than 0.55 eV could not fit the temperature data. The capacitance measured is thus presumably the signature of a state or group of states that lies within 0.19 eV of the metal Fermi level.

To reduce the number of unknown variables, an effective single level opposite the metal Fermi level which captures electrons mainly from the conduction band and emits mainly to the metal was assumed. The best match for the as-deposited data is then as shown in Fig. 12. A small shift in the concentration N_T and time constant product $\sigma_n \tau_E$ was needed to fit the experimental curves over the measured temperature range as shown. For the annealed sample, the theoretical model and experimental data match quite well with a single value of N_T and $\sigma_n \tau_E$ as seen in Fig. 13. Upon annealing the density of the effective level decreases by a factor of 2.3, from 1.25×10^{12} to $0.54 \times 10^{12}/cm^2$, while the time constant product increases by 2.6. This decrease in concentration is consistent with the movement of the interface into the silicon upon the formation of silicide. The original interface presumably has many extrinsic impurities which do not exist at the new interface.

The necessity in using small shifts in the state parameters in order to match the data indicates the single level model is not entirely correct. After annealing, however, the distribution probably moves closer to this model as evidenced by the fit achieved using only a single parameter set. Once again, a

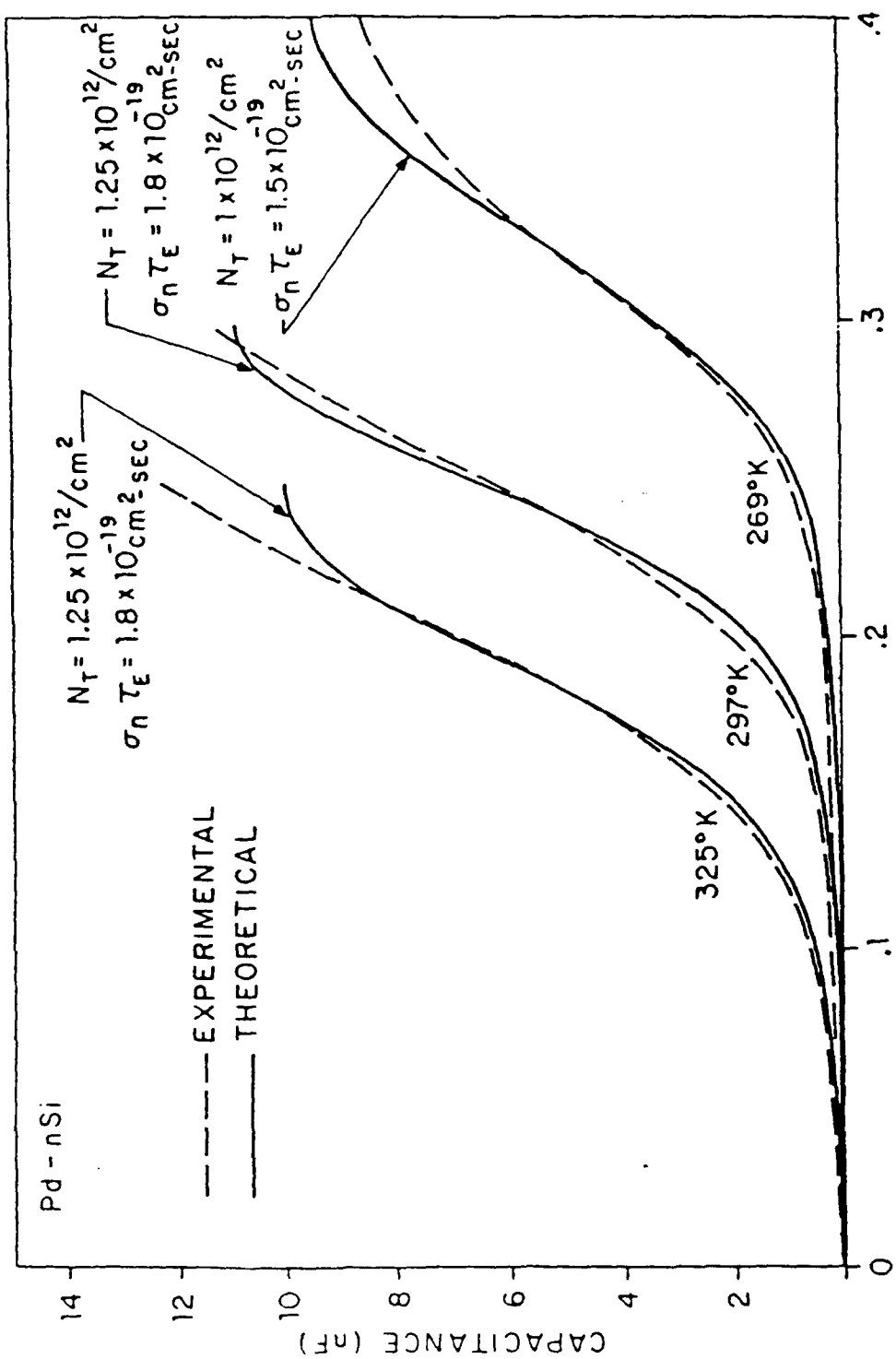


Figure 12. Match between theoretical prediction, using a single interface level opposite the metal Fermi level with the parameters shown, and the experimental results for the as-deposited diode at 269, 297, and 325 K.

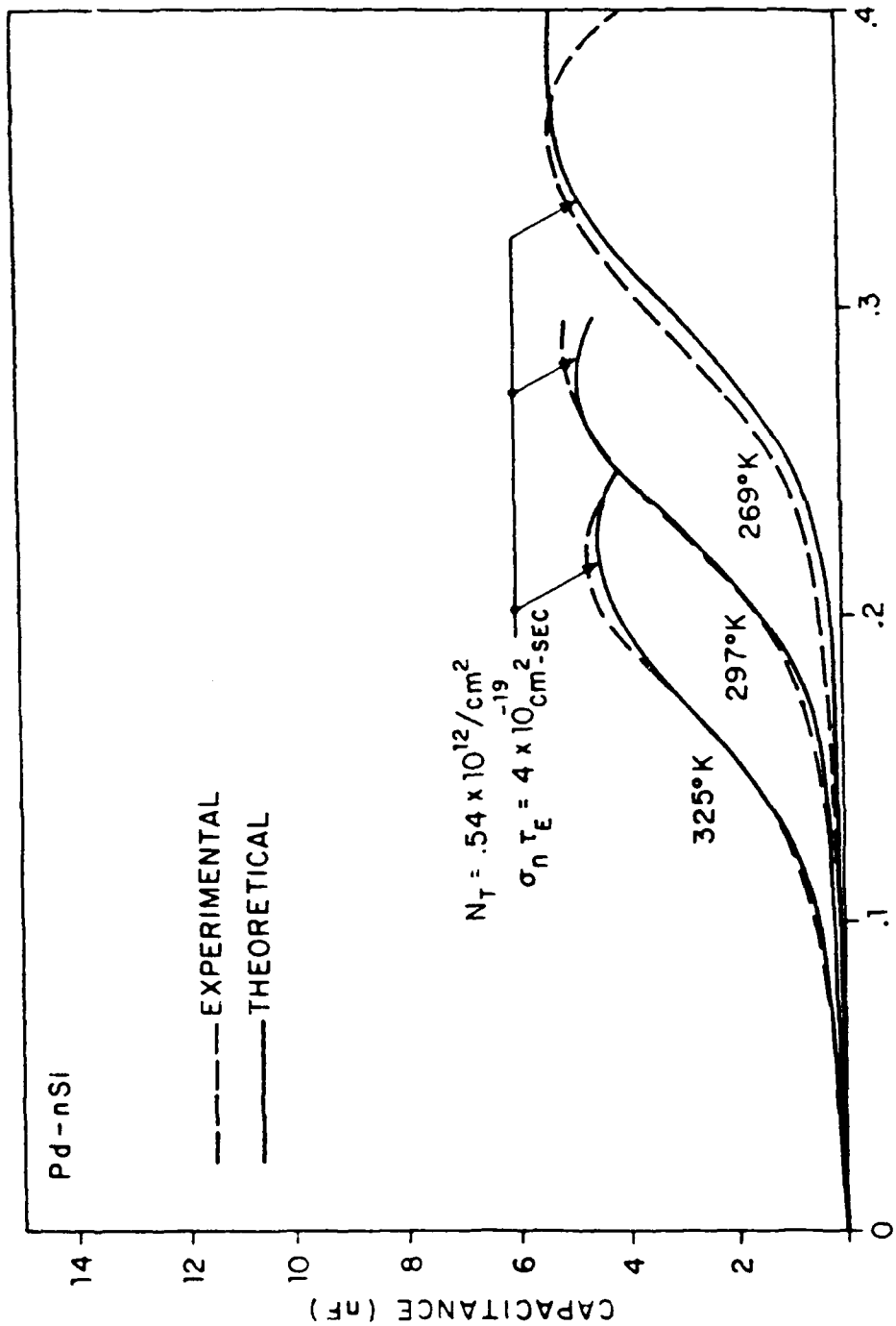


Figure 13. Match between theoretical prediction, using a single interface level opposite the metal Fermi level with the parameters shown, and the experimental results for the annealed diode at 269, 297, and 325 K.

band of states which decreases in width upon annealing is consistent with theories on silicide formation.

Using this preliminary model, the capacitance data for the palladium silicon diode is the signature of a state opposite the metal Fermi level. This proposed effective single level, or the band of states which it represents would be responsible for the barrier height in the contact. Upon junction formation, the semiconductor bands bend until the Fermi level crosses the location of the state. Then any additional charge that needs to flow into the metal to achieve equilibrium will come from the changing occupancy of the state and the Fermi level will be pinned at this position. It is not possible to determine whether the state is initially present on the silicon surface or induced during the nucleation and deposition processes.

Although able to match the temperature dependence of the data, this model neglects the capacitance due to the modulation of the thermionic emission current by the variation of interface charge. It is found that for a given interface state distribution, this capacitance is greater than the one described above. We can understand the origin of this capacitance by proceeding as follows. The Schottky barrier current can be written as

$$I = AA^{*}T^{2} exp\left\{ - \frac{q}{kT} \left| \Phi_b + \Phi_s - V + R_s I \right| \right\}, \qquad (20)$$

where Φ_s and R_sI represent the voltages dropped across the interface and the semiconductor bulk, respectively. If a small ac signal, ΔV, is present in addition to the dc bias, both Φ_s and R_sI will change and an ac current, i, will be observed. Simply applying Eq.(20), we have

$$I + i = I \exp\left\{ \frac{q}{kT} \left| \Delta V - \Delta\phi_s - R_s i \right| \right\}, \tag{21}$$

where $\Delta\phi_s$ and $R_s i$ are the resulting variations of ϕ_s and $R_s I$. The diode admittance is then given by

$$Y = \frac{i}{\Delta V} = \frac{qI}{kT} \frac{(1 - \Delta\phi_s / \Delta V)}{kT(1 + qR_s I/kT)} . \tag{22}$$

The variation of the interface potential, $\Delta\phi_S$, originates mainly from charge accumulation at the contact. This process is not completed instantaneously; it requires a certain period of time, depending on both carrier capture and emission rates. Letting ΔV_{s_R} and ΔV_{s_I} be the real and imaginary parts of $\Delta\phi_s$ the diode conductance and equivalent parallel capacitance are then given by

$$G = \frac{qI}{kT} \frac{(1 - \Delta V_{sR} / \Delta V)}{(1 + qR_s I/kT)} , \tag{23a}$$

$$\omega C = \frac{qI}{kT} \frac{(- \Delta V_{sI} / \Delta V)}{(1 + qR_s I/kT)} . \tag{23b}$$

By Gauss' law

$$\Delta\phi_s = - \frac{\delta}{\varepsilon_s} \Delta Q_t = - \Delta Q_t / C_i , \tag{24}$$

The variation of total charge, ΔQ_t, contains two components, ΔQ_{ss}, due to interface charge, and ΔQ_{sc}, due to the depletion layer charge. In most practical situations ΔQ_{sc} is much smaller than ΔQ_{ss} so Eq. (24) can be simplified to

$$\Delta\phi_s = - \frac{\Delta Q_{ss}}{C_i} . \tag{25}$$

The variation of interface charge arises from the variation of electron occupany at the interface. It can be calculated from the following integral:

$$\Delta Q_{ss} = -q \int N_{ss}(E)\,\delta f(E)\,dE \tag{26}$$

where $\delta f(E)$ represents the increment of occupany probability at the interface state level E due to the ac current flow, and $N_{SS}(E)$ is the density of states at the corresponding energy level. The occupancy probability of a state is given by Shockely-Read-Hall statistics as discussed previously. The variation of occupancy upon application of the small signal can be easily be determined by differentiation. If we denote $N_s(E_f^s)$ by

$$N_s(E_f^s) = \int_{E_F^m}^{E_f^s} N_{ss}(E)\,dE \tag{27}$$

where E_F^m represents the Fermi level in the metal and E_F^s the quasi Fermi level in the semiconductor we end up with the following expression for the capacitance

$$\omega C = \frac{q^2 I}{kT(1 + qR_s I/kT)} \frac{N_s(E_f^s)}{C_i \Delta V} \frac{\omega(1-f)4\sigma_n j/q}{(4\sigma_n J/q + 1/\tau_m)^2 + \omega^2} \tag{28}$$

j is the small signal current density which can be obtained directly from the conductance .

Two nickel silicide diodes were prepared in a UHV environment[14] to test this theory. One had an epitaxial interface of Type B, and the other has a non-epitaxial A/B mixed type interface.[15] The sample diodes were fabricated by e-beam evaporation of nickel onto a clean Si(111) surface, with a Ti ohmic back contact. The barrier height of these diodes was measured by I - V method and was found to be 0.77 eV for the epitaxial and 0.66 eV for the non-epitaxial sample. Forward bias capacitance measurements were made over a

range of temperature and frequency using differential voltage capacitance spectroscopy. At each temperature σ_n and τ_m can be determined by noting the peak position in the capacitance versus volage plot at a given frequency and in the capacitance versus frequency plot at a given voltage. It was assumed that δ = 5 A and $\varepsilon_i = \varepsilon_0$. As the temperature goes down σ_n decreases while τ_m increases as shown in Table 1. The integrated density of states, $N_S(E_f^s)$ is chosen by matching the peak height at a given temperature. The resulting correlation between the experimental data and the theoretical model is demonstrated in Fig. 14. If the states are assumed to be distributed within the first few angstroms of the semiconductor so that the time constant for emission to the metal is dispersed the theoretical peak is broadened and better matches the experimental data. By matching the peak height at various temperatures, $N_{ss}(E_f^s)$ can be determined for different positions in the bandgap. The actual density of states, $N_{ss}(E)$, can then be found by differentiating $N_{ss}(E_f^s)$ with resepect to E_f^s. The results of such a calculation for the epitaxial (Type B) and non-epitaxial (Type A/B) nickel silicide are shown in Fig. 15.

The differences in spectrum between the B-type and the mixed A/B-type devices are quite evident: although both display a peak, the densities of states are very different. The peak density for the non-epitaxial device is 6.1 $\times$ 10^{12}/eV-cm^2. This number is almost one order of magnitude greater than that for the epitaxial device. The density peak in the epitaxial device lies approximately 0.12 eV above that of the non-epitaxial device. This is the same as the barrier height difference of the two diodes. It indicates that most

Parameter	Device Type	300 K	270 K	240 K	210 K
τ_m (sec)	B	1.5×10^{-5}	2.6×10^{-5}	4.2×10^{-5}	5.6×10^{-5}
	A/B	1.1×10^{-5}	1.6×10^{-5}	2.8×10^{-5}	1.2×10^{-4}
σ_n (cm^2)	B	4.0×10^{-14}	7.0×10^{-15}	5.5×10^{-15}	4.8×10^{-15}
	A/B	6.8×10^{-15}	2.2×10^{-15}	1.0×10^{-15}	7.0×10^{-16}

Table 1. Interface state parameters obtained using the single time constant model.

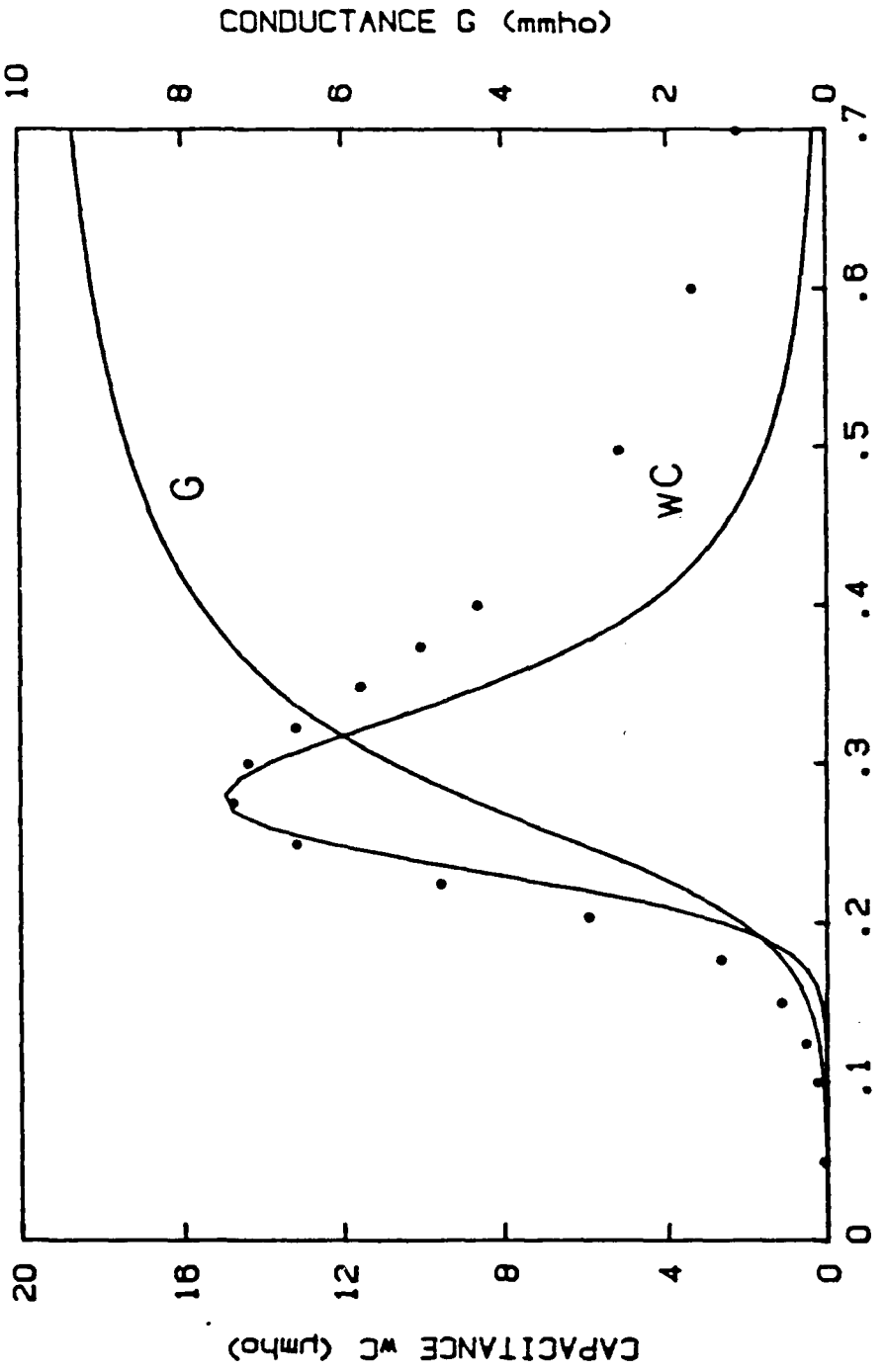


Figure 14. Capacitance (wC) and conductance (G) as a function of bias for the A/B type device. The conductance curve and the dots are experimental data measured at 270 K and 108 Hz, and the solid line, wC, is the result calculated from the single time constant model.

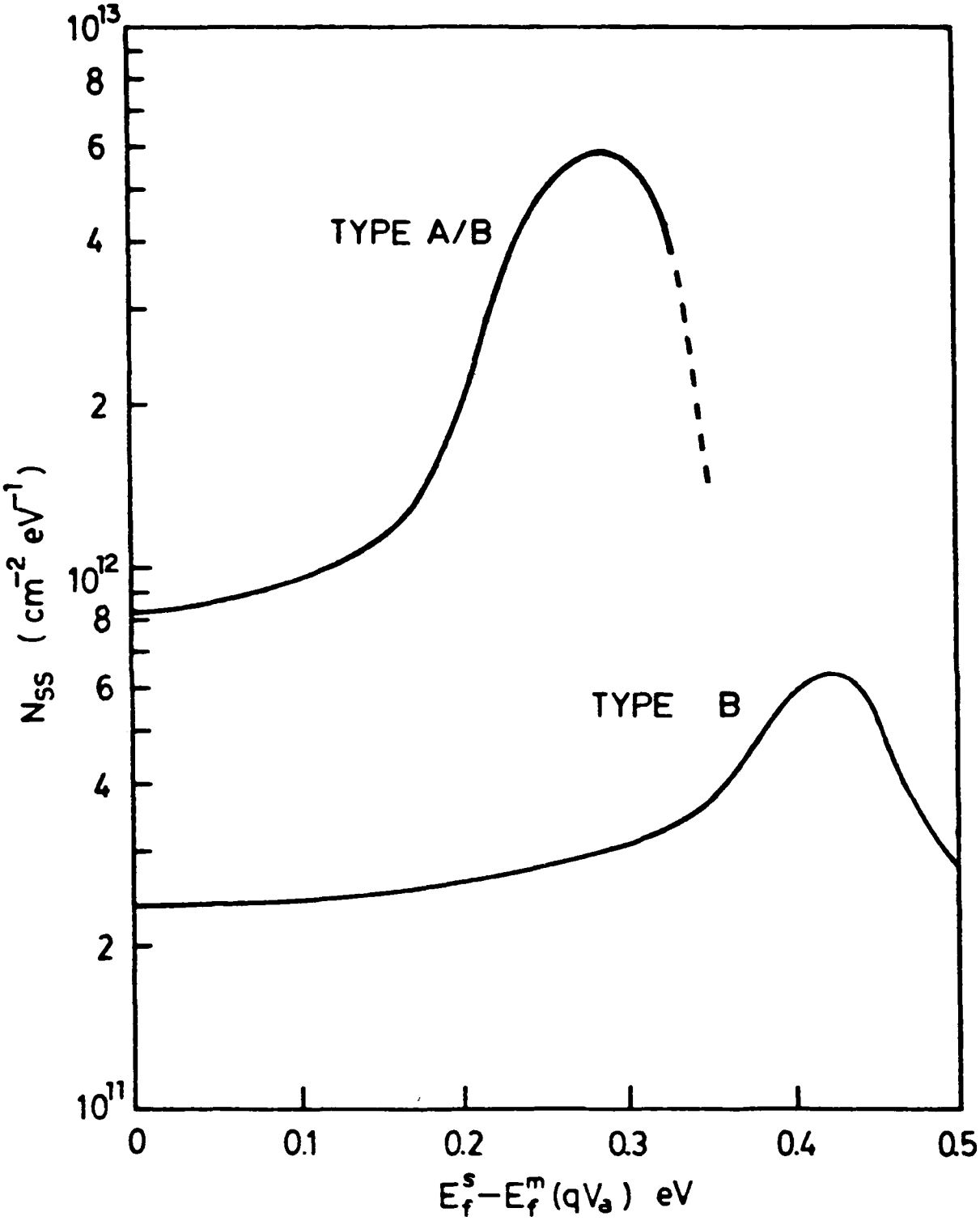


Figure 15. Spectra of interface state density. Note the difference in density between the epitaxial and nonepitaxial devices.

of the states in the two devices are located at a same energy position - 0.35 eV below the conduction band. Therefore, they result from the same interfacial mechanism. A measurement on an epitaxial Type A device revealed that its density of inteface states is bascially the same as seen in Type B devices. Type A and Type B devices are both epitaxial $NiSi_2$, but differ in lattice orientation. This leads us to believe that the interface trap states are likely to be associated with lattice defects, which is consistent with TEM observations, where the non-epitaxial samples always display a higher degree of lattice imperfections.

Both of the models used to explain the forward bias capacitance assume that minority carrier effects can be ignored. Schottky diodes are considered to be majority carrier devices with negligible influence from minority carriers. However, it must be remembered that our technique is for measuring a device component orders of magnitude smaller than the majority carrier conductance. Numerical simulations by Green and Shewchun[16] demonstrated the dependence of the imaginary component of the Schottky diode admittance on both forward bias voltage and frequency. In the frequency regime used in our measurements the susceptance was seen to be capacitive at low voltage and becomes inductive as the voltage is increased. The capacitance is the usual minority carrier diffusion component while the inductance is due to modulation of the conductivity in the quasi neutral region by the injected minority carriers. These positive and negative regimes are similar to those we have seen in previous measurements. However, the maximum capacitance reported by Green and Shewchun is two orders of

magnitude smaller than our measured results and occurs only in samples with higher barrier heights.

We attempted to enhance the theoretical value of the minority carrier diffusion capacitance by introducing an imperfect back contact. This is similar to the work of Scharfetter[17] who looked at injection efficiency and charge storage but did not evaluate any capacitance. Our model assumes that the minority carrier quasi-Fermi level is flat across the depletion region and pinned at the metal Fermi level at the interface. The minority carrier stored charge at the edge of the depletion region is then given as

$$p(W) = p_{no} e^{qV/kT} \tag{29}$$

where p_{no} is the equilibrium concentration of minority carriers and V is the applied voltage. The boundary condition at the back contact is written in terms of a surface recombination velocity for minority carriers, σ, as

$$j(L) = q\sigma p(L) \tag{30}$$

The steady state distribution of minority carriers in the quasi-neutral region is found as a function of L, σ, and the minority carrier lifetime, τ_p, by solving the minority carrier continuity equation. The carrier concentration can be summed over the length of the quasi neutral region to find the total stored charge. The low frequency diffusion capacitance is then evaluated as the difference in stored charge at two voltages divided by the infinitestimal change in voltage. Computer software was developed to calculate and plot the resulting theoretical capacitance with the length of the quasi-neutral region, the minority carrier lifetime, and the back contact recombination velocity as variable parameters. The electric field in the quasi neutral region, needed in

the program, is expressed in terms of the majority carrier current and is taken from actual I-V data of Pd n-n$^+$ Si-Pd structures. The n$^+$ substrate results in the formation of a good ohmic contact for majority carriers while the n on n$^+$ barrier blocks the flow of minority carriers. The recombination velocity for minority carriers is not infinite and depends on the doping ratio between the n and n+ region. The length of the epitaxial layer was 25 μm with ρ = 7.8 Ωcm while the total Si thickness was on the order of 300 μm and the substrate resistivity approximately 0.003 Ωcm.

The minority carrier diffusion capacitance was found to be very dependent on the value assumed for σ. By varying σ from infinity (perfect recombination) to 0 (perfect blocking) the maximum capacitance in the voltage range investigated increased by a factor of twenty. However, the values were still much less then the experimental results. In addition, a significant capacitance could only be achieved when the minority carrier diffusion length was less than or on the order of the quasi neutral region. For our sample this would require a minority carrier lifetime in silicon less than 10^{-6} sec. Evidence thus indicates that minority carriers cannot be responsbile for the observed positive capacitance and can safely be neglected.

P-n junctions on the other hand are true minority carrier devices. Since our measurement techniques do not depend on any property specific to Schottky barriers they can be applied equally well to pn junctions. We found a useful application for the measurement of the forward bias capacitance of a pn junction in the polyemitter transistor problem. It has been noted that the gain of a silicon npn bipolar transistor can be increased by placing a layer of

polysilicon between the monocrystalline silicon emitter and the metal contact and then using this layer as a doping source for the emitter. This phenomenon has been explained by another group in our laboratory as due to electrically active arsenic segregating at the interface between the polycrystalline and monocrystalline silicon and blocking the minority carrier current flowing from the base into the emitter contact. If this explanation is correct then minority carrier "storage" in the emitter will increase, and the capacitance due to these charges will be enhanced. It is difficult to measure this capacitance in the transistor structure due to the heavy doping of the emitter. A pn junction diode was constructed as shown in Fig. 17 to simulate this effect. The n region represents the transistor's emitter, while the p^+ region corresponds to the base. Devices with and without the polysilicon layer between the n region and the metal contact were fabricated. Under forward bias the diffusion capacitance is due mainly to minority carriers in the lightly doped n region. Using our accurate phase capacitance spectroscopy, it was possible to measure this forward bias diffusion capacitance. Upon making this measurement we found that the capacitance in the presence of the polysilicon contact was greatly enhanced as shown in Fig. 18. This is evidence for the blocking of minority carriers by the poly layer demonstrating that the segregated arsenic is electrically active, a result that cannot be obtained by traditional SIMS measurements.

In summary, we have developed and utilized a technique facilitating the measurement of capacitance in the presence of a much larger conductance. A "fourth quadrant" for device characterization is now available in addition to

P+/N DIODES

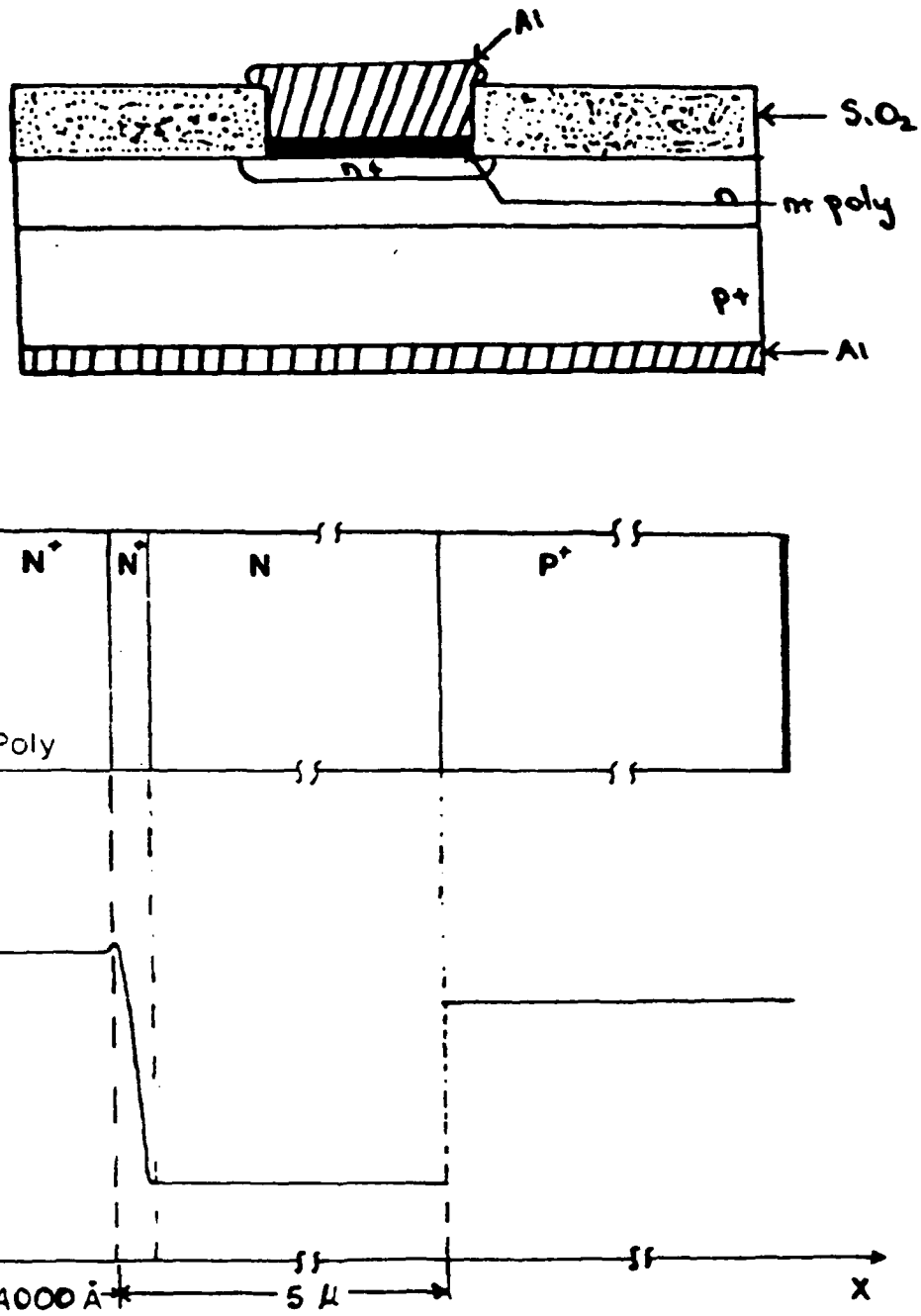


Figure 17. P-n junction diode used to simulate the base emitter region of a polyemitter transistor.

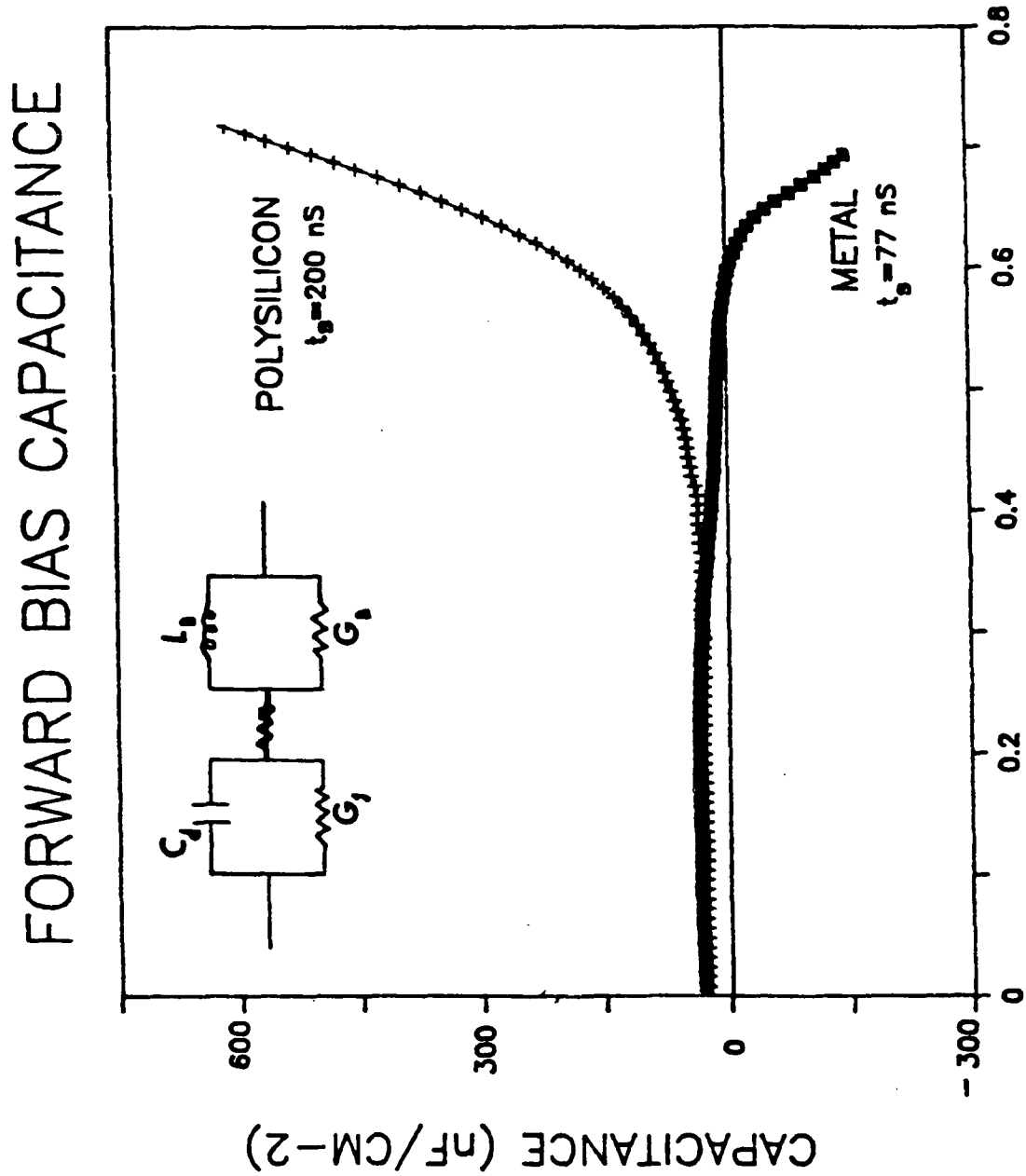


Fig. 18. Forward bias capacitance for diodes with and without the polysilicon layer.

the routine forward and reverse bias current and reverse bias capacitance methods. Experiments using this added capability enable us to determine the interface state distribution in Schottky diodes and minority carrier effects in pn junctions. For silicon Schottky barriers we have detected a decrease in the number of interface states upon formation of silicide and a correlation between interface state density and structural perfection. The density of states has been shown to be on the order of $10^{13}/cm^2$. We feel that with continued work in this area many interesting results will be forthcoming and the understanding of metal-semiconductor contacts greatly enhanced.

Chapter 2 - Controllable Schottky Barrier Heights on GaAs

Schottky barriers on gallium arsenide have been the subject of extensive investigation for the last decade. For the GaAs (100) surface, Schottky barrier heights correlate only weakly with the work function of the metal. This has led to the conclusion that the Fermi level is pinned at this interface due to a high density of bandgap states[18] or the presence of excess arsenic[19]. When an interface contains a high density of electronic states, this will dominate the barrier formation, allowing differences in the metal semiconductor work function to play only a small role in determining the magnitude of a Schottky barrier. For the GaAs (100) surface Schottky barrier height correlate only weakly with the work function of the metal. If the GaAs surface can be modified to change the density of interface states the Schottky barrier which results would be more influenced by the metal work function. In the work reported in this chapter we have used photochemistry to alter the GaAs (100) surface through the reaction of oxygen under deep UV illumination prior to metal deposition and have investigated the electrical characteristics of the resulting contacts.

Previous studies of the effect of thin oxide layers on the electrical properties of Schottky contacts found that for a variety of metals, the Schottky barrier increases. In those studies the oxide layer was formed by prolonged exposure to wet oxygen[20] or by an aqueous chemical reactions.[21] Oxides formed on GaAs in moist ambients are different from those grown in dry oxygen, probably due to the incorporation of hydroxyl groups in the oxide. Therefore, the effect of the oxides used in our study, formed in dry oxygen,

would be expected to be different from the previous studies. In the previous studies, trapping of charge at the interface or in the oxide is believed responsible for the observed increase in barrier height. Chang, et al[23], have suggested that a suitably chosen chemical reaction could allow the formation of an oxide on GaAs which would not cause the creation of charge traps.

Another group in our laboratory has reported that deep UV light greatly enhances the rate of oxidaton of GaAs surfaces compared to dark oxidation or oxidation with near UV light exposure.[24] The mechanism responsible for this enhancement is not completely understood, but it is generally agreed that the enhancement is at least in part due to a carrier related effect.[25,26,27] Recent studies indicate that the deep UV enhancement seems to involve the photodissociation of an O_2^- species formed by photogenerated carriers.[28] Thin oxide layers formed in this way have been found to be stoichiometric with respect to Ga and As. Oxide layers which are nonstoichiometric have also been formed by annealing after oxide growth. This results in a surface which is Ga-oxide rich, as will be shown later. Metal contacts were deposited on both stoichiometric oxide and Ga-oxide rich surfaces. The variation in Schottky barrier height for various metal contacts formed on oxidized surfaces was found to depend much more strongly on the work function of the metal overlayer than is observed on clean GaAs surface. It is concluded that a more ideal relationship between metal work function and Schottky barrier height exists for the oxidized surface than occurs for clean GaAs surfaces.

The experiments in this study were performed in a modified Leybold-Heraeus surface analysis system which consists of two chambers isolated by differentially pumped seals around a sample rod. This allows one chamber to be filled with O_2 to 100 Torr, while the other chamber remains under UHV. A sample can be moved between these two chambers in a matter of moments to allow surface anlaysis only a short time after sample processing. Typical base pressures are 1×10^{-10} Torr in the analysis chamber and 3×10^{-7} Torr in the preparation chamber. The preparation chamber has been modified to allow UV light exposure of a sample through a Suprasil window and metal deposition from an electron beam evaporation source. The evaporation source is in a chamber isolated from the preparation chamber by a gate valve which acts as a shutter during metal deposition. The source to sample distance is 30 cm. The acceleration potential of the electron beam evaporator is 4 kV. A crystal thickness monitor is used to control metal deposition rates and final thickness. The typical metal deposition rate is 3 A/sec. The GaAs used in this study was (100) oriented, horizontal Bridgman grown and nominally undoped with $n = 1 \times 10^{16}$ cm^{-3}. All samples were degreased by sequentially soaking in hot trichlorethylene, acetone, and methanol. They were then chemically etched for 15 seconds in $NH_4OH:H_2O_2:H_2O$ (1:1:10), oxidized in $H_2SO_4:H_2O_2:H_2O$ (10:1:1) for 1 minute, quenched in 10^{20} Ω-cm water, and blown dry with N_2. A sample was then mounted on a Mo plate with melted In and immediately inserted into the UHV system, where it was heated in vacuum to 550 °C for 5 minutes. This desorbed the oxide layer formed during cleaning and served to anneal the In on the back of the sample, providing an

ohmic contact for electrical measurements. Waldrop has performed LEED studies to show that a similar cleaning procedure provides a clean, well ordered surface.[29]

After the surface had been cleaned and XPS performed, very pure O_2 was leaked into the preparation chamber, typically to a pressure of 10 Torr. Details of the surface oxidation procedure have been reported in Ref. (22) and (24). Deep UV irradiation of the GaAs was performed with a low power, high repetition rate KrF excimer laser (λ = 248 nm) of photon energy 4.8 eV. Typical laser power used is < 2 mJ/cm2 so that thermal effects are negligible (transient surface heating < 50°C expected).

Oxide thicknesses were measured using XPS by determining the ratio of areas under the oxidized As peak to the As peak from the substrate. Then, using the substrate signal attenuation through the oxide layer, a good estimate of the oxide thickness can be made from the escape depth of the electrons. We have made the common assumption that the electron escape depth through an oxide layer is the same as through the substrate, namely, 7 A for the As 2p3/2 signal at ~ 163 eV kinetic energy and 25 A for the As 3d signal at ~ 1445 eV kinetic energy. The Ga signal is not used because there is only a small chemical shift between the oxidized Ga signal and the substrate Ga signal, making a determination of area under each peak very imprecise. Oxide thicknesses between 3 and 50 A can be accurately controlled by varying the O_2 pressure and duration of irradiation. It is interesting that the oxide thickness depends much more on the time of photon exposure than on the O_2 pressure in the chamber. This suggests that photogenerated carriers play a

rate limiting role in the enhanced oxide growth mechanism. A 3 A oxide can be reproducibly formed with a 5 min irradiation, while a 15 A oxide will form in 20 min of irradiation.

The oxides used in this study are between 3 and 10 A thick in order to produce contacts with good ideality factors. The oxides grown in the manner described above are found by XPS to be stoichiometric with respect to Ga and As, consisting predominantly of Ga_2O_3 and As_2O_3.[24] However, we have also formed nonstoichiometric oxides. Using the known fact that Ga_2O_3 is more thermally stable than As_2O_3, we can produce a Ga-oxide rich surface by annealing the oxidized GaAs. After a stoichiometric oxide is grown, and the chamber has been re-evacuated, the sample is heated to 500°C[30] for 10 min and allowed to slowly cool. This is believed to cause a reaction where As_2O_3 reacts with the substrate to form Ga_2O_3 while As desorbs from the surface.

Typical XPS data is shown in Fig. 19 comparing a surface with a stoichiometric oxide to the same surface after annealing. The As $2p_{3/2}$ peak indicates that the oxide layer is 6 A thick before annealing. Notice that after annealing, there is very little signal from the chemically shifted peak due to oxidized As. Since the Ga peak cannot be used to determine the thickness of the oxide layer, we used the preannealed oxide thickness as a measure of the amount of oxygen on the GaAs surface before metal deposition. The Ga peak after annealing, however, is still chemically shifted 0.9 eV from the substrate peak position, characteristic of oxidized Ga. The ratio of the As $2p_{3/2}$ signal to the Ga $2p_{3/2}$ signal for the annealed surface is 0.46, in agreement with the prediction that the surface is Ga-rich . The ratio for a stoichiometric surface

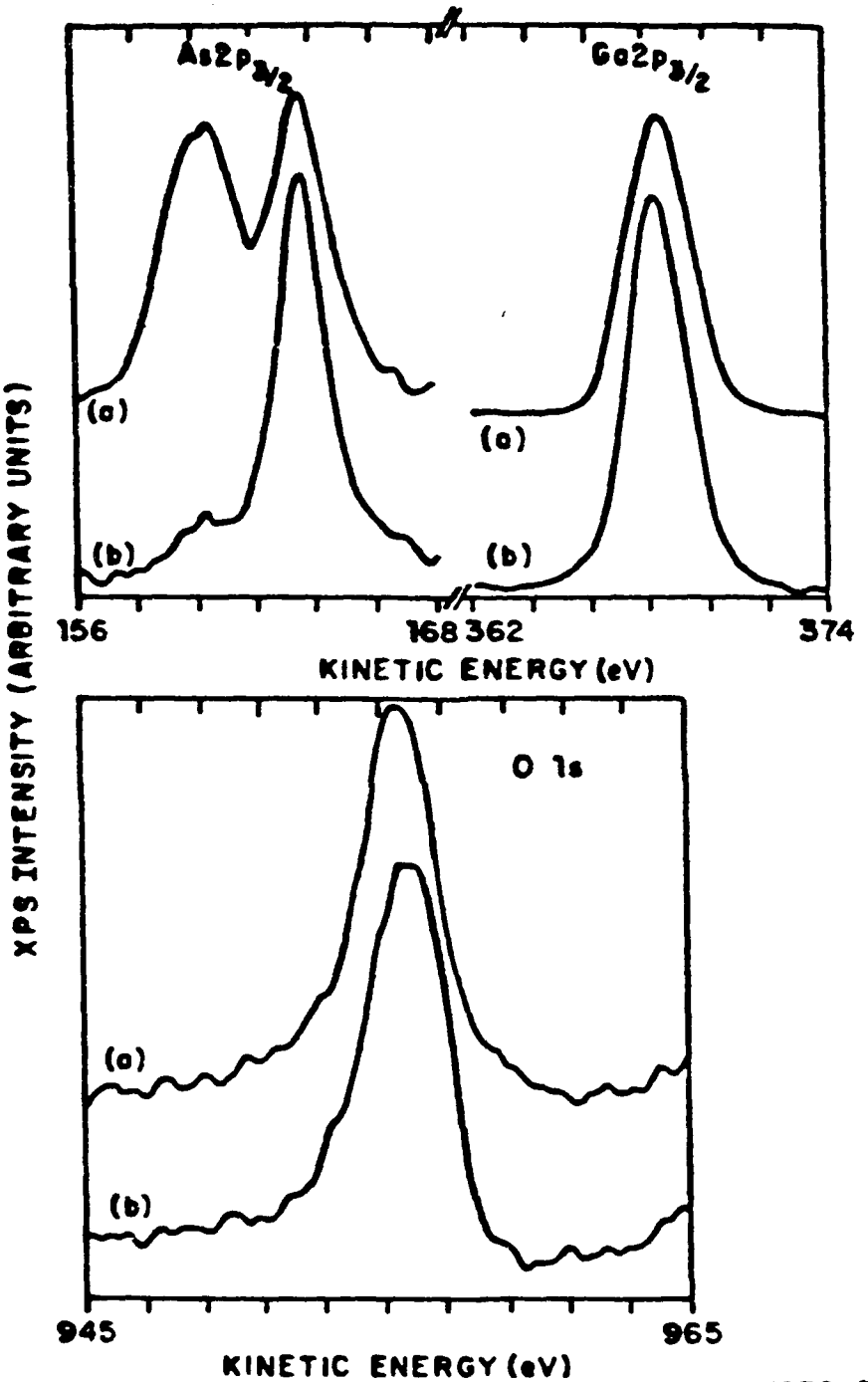


Figure 19. X-ray photoelectron spectroscopy data for GaAs surfaces (a) with stoichiometric oxides, and (b) the same surface after annealing 10 min at 500 C. The oxidized As signal is shifted to lower kinetic energy. The curves labeled (b) show a Ga oxide rich surface. Note the O 1s peak has the same magnitude before and after annealing. The data has been smoothed and the background has been subtracted in all cases.

has been found from MBE prepared samples to be 1.4.[31] Notice in Fig. 19 that the O 1s peak is unchanged in magnitude before and after annealing, consistent with our assumption that the amount of oxygen on the surface does not change during annealing.

The metals used to form contacts in this study were Pd, Cu, Cr, and Ti. They were chosen because they have different reactivities with GaAs oxides, they cover a range of metal work function values, and all have been found to react strongly with GaAs surfaces.[32,33,34] Pd and Cu are inert to an oxide layer on GaAs, while Ti and Cr react completely with the oxygen in thin oxide layers.[35] The contacts were formed by evaporation through a thin Mo mask pulled close to the sample surface just prior to deposition. The contacts were dots of 8×10^{-3} cm^2 area with at least six contacts per sample. After metal deposition, the sample was removed from the UHV system and the contacts were electrically characterized by dark current votlage (I-V) and internal photoemission (PE) measurements.[36]

The results of electrical measurements for the various metals on the different surface oxides, as well as on clean control samples, are summarized in Table 2. The results are typical values from measurements of several contacts of each category. The optimum oxide thickness to cause the maximum change in Schottky barrier height for each metal was not investigated. It can be seen that an oxide layer reduced the barrier height for Cu, Cr, and Ti, but increased the barrier for Pd. It will be discussed below that this correlates with the work functions of the various metals. It is also clear that the contacts with Ga-rich oxide layers produced a larger barrier height

Table 2. Schottky barriers on n:GaAs for clean interfaces, UV formed oxide interfaces, and annealed oxide interfaces.

Metal	Surface Preparation	Oxide Thickness (A)	PE Barrier (eV)	I-V Barrier (eV)	Ideality factor
Pd	Ref.			.87	1.03
	Clean	0	.85	.86	1.03
	Stoichiometric Oxide	3.0	-	.92	1.04
	Stoichiometric Oxide	5.0	.87	.92	1.04
	Ga-rich Oxide	6.8	.93	.93	1.04
Cu	Ref.			.92	1.05
	Clean	0	-	.88	1.05
	Stoichiometric Oxide	4.2	.84	.84	1.24
	Ga-rich Oxide	4.2	.65	.77	1.03
Ti	Ref.			.79	1.03
	Clean	0	.74	.78	1.02
	Stoichiometric Oxide	7.2	.72	.65	1.02
	Ga-rich Oxide	7.1	.70	.63	1.00
Cr	Ref.			.73	1.04
	Clean	0	.70	.73	1.05
	Stoichiometric Oxide	7.5	.68	.62	1.08
	Ga-rich Oxide	6.0	-	.54	1.07

Ref. values from J.R. Waldrop, Appl.Phys Lett. 44,1002(1984), J.R. Waldrop, J. Vac. Sci. Technol. B2, 445 (1984)

Oxide thickness +- 10% ; I-V and PE barriers +- .01 eV

variation for the various metals and better ideality factors from I-V measurements. The better ideality factor is especially noticeable for the Cu contacts. For Cu contacts, similar stoichiometric oxide thickness and Ga-rich oxide thickness result in a much better ideality factor for the Ga-rich contact.

The barrier heights in Table 2 measured by internal photoemission agree with the trends observed in the I-V measurements. This is important since PE measurements are the most direct measure of barrier heights,[36] not dependant on contact area, physical constants, or low barrier height regions. In some cases, PE measurements could not be made. The variaiton in PE barrier heights on clean surfaces for different metals is only 0.15 eV, while on Ga-rich oxide surfaces the variation is 0.28 eV. The increase in barrier height variation is even greater from
I-V measurements. From these it is seen to vary 0.39 eV for Ga-rich oxide surfaces, compared to only 0.12 eV for contacts on clean surfaces. This corresponds to ~ 25% of the GaAs bandgap, compared to ~ 8% for the clean surfaces examined here.

I-V data from each of the metals and surface treatments is shown in Figs. 20 and 21. For the metals reactive with oxygen, Cr and Ti, the shift of the I-V plot is very similar, see Fig. 20. The stoichiometric oxide shifts the current significantly higher, while the shift for a Ga rich oxide is even greater. These shifts indicate a decrease in Schottky barrier height. In all cases, the plots are parallel, indicating no change in contact ideality. It was found that the oxide thckness had less of an effect on the contact ideality factor for metals reactive with oxygen than for metals inert to the oxide layer.

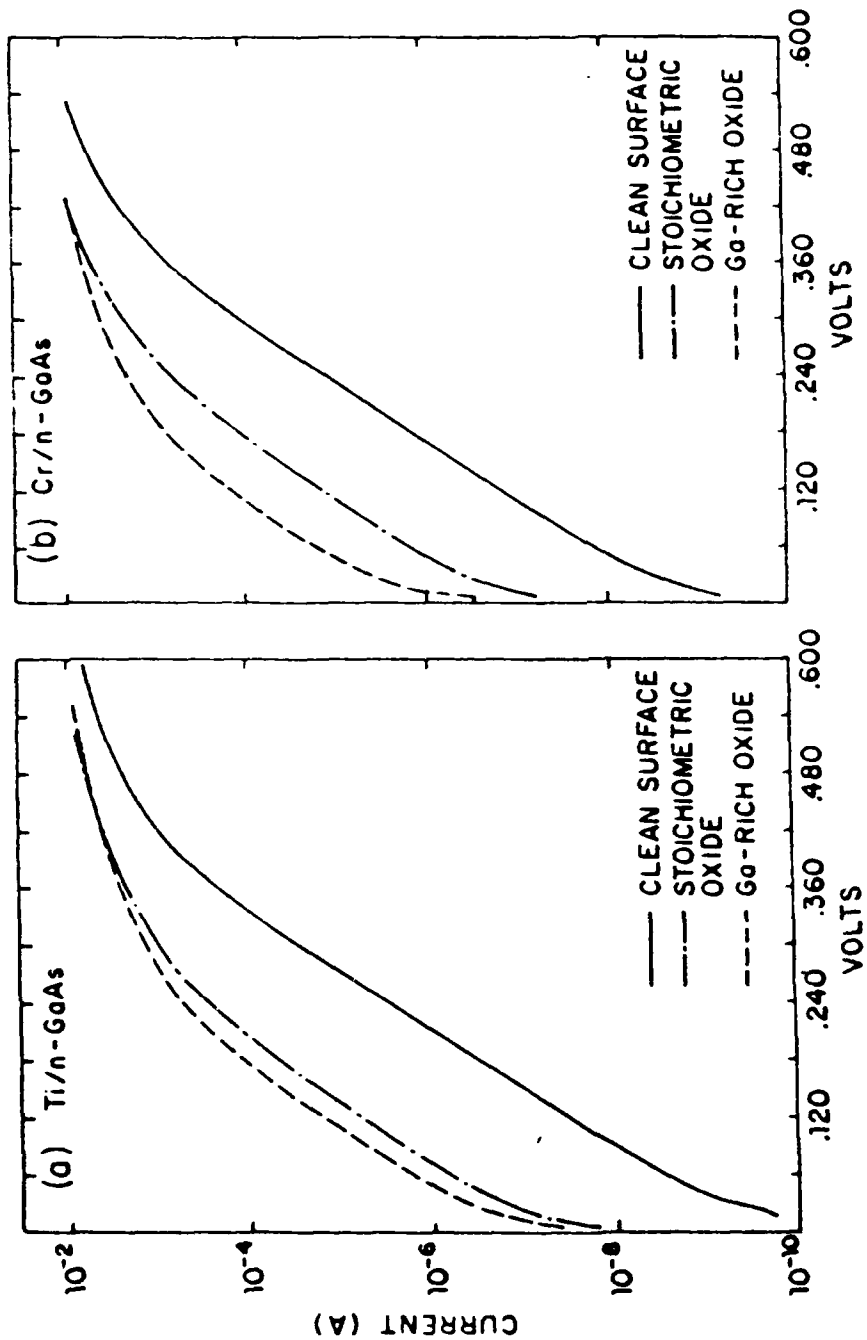


Figure 20. Natural log of the current versus applied voltage for the metals reactive with a GaAs-oxide layer.
(a) Ti on n-GaAs with the indicated surface treatments
(b) Cr n-GaAs with the indicated surface treatments.

This could be of practical importance in making contacts to oxidized surfaces. For the Cu contact, Fig. 21(a), a stoichiometric oxide only slightly shifts the plot to higher current, indicating lower barrier, but it also degrades the contact ideality. Cu contact idealities were the most strongly affected by the stoichiometric oxide layers of the contacts in this study. For a Ga-rich oxide, however, the plot shifts to that for a much lower barrier with good ideality.

The behavior for Pd contacts is the opposite of that for the above metals. Fig. 21(b) shows that a stoichiometric oxide shifts the I-V plot downward, corresponding to a higher barrier height. This plot indicates no degradation of contact ideality, but this is true only for oxides less than 7 A thick. Thicker oxides increase the ideality factor for the contact, and produce lower apparent barrier heights. Fig. 21(b) also shows a further increase in barrier height for Pd on a Ga-rich oxide surface with the ideality factor restored to the original value. While this further increase in barrier height is slight, it was consistently observed.

The large increase in the range of Schottky barrier heights for contacts formed on surfaces which have been oxidized using deep UV irradiation at room temperature suggests that the density of interface states has been changed, allowing the metal work function to play a larger role in the barrier formation. In Fig. 22 the Schottky barrier height for the various contacts have been plotted versus the work function of the contact metal. Also shown are the barrier height expected if the Fermi level is completely pinned and the ideal barrier height limit in the absence of interface states. In all cases, the change in barrier height for contacts on oxidized surfaces is toward the ideal

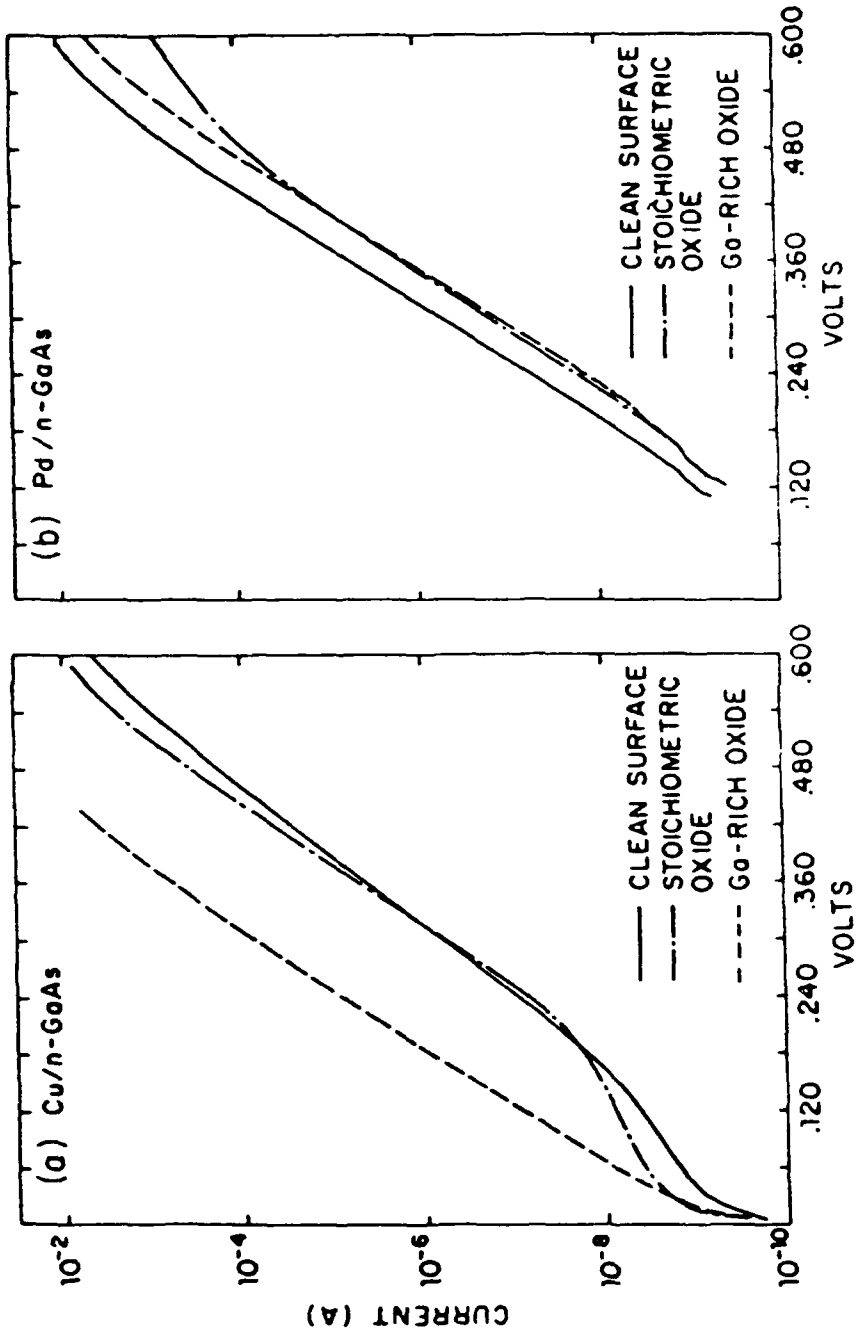


Figure 21. Natural log of the current versus applied voltage for the metals inert to a GaAs-oxide layer. (a) Cu on n-GaAs with the indicated surface treatments, (b) Pd on n-GaAs with the indicated surface treatments.

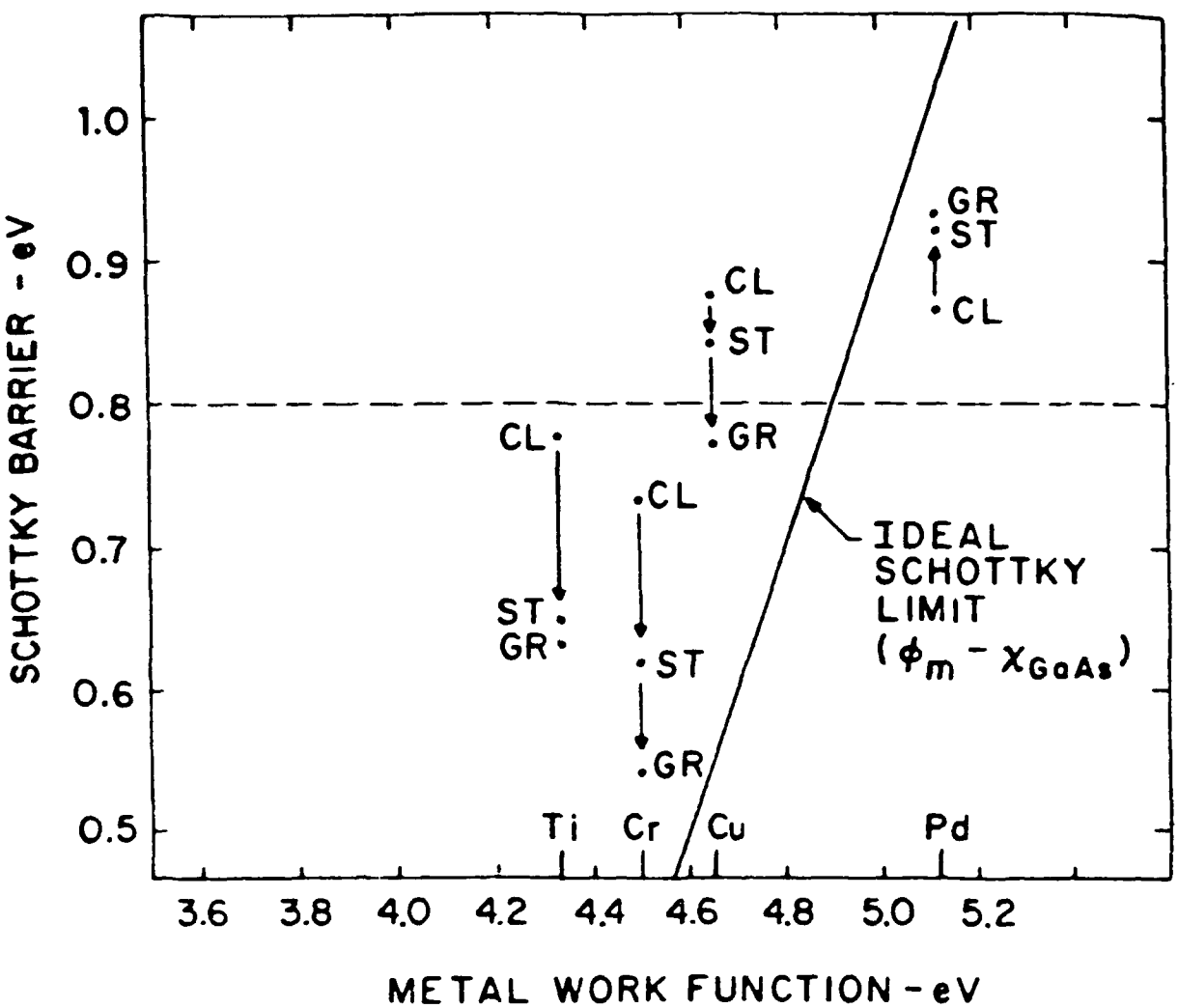


Figure 22. Schottky barrier height versus metal work function. Also plotted, is the ideal Schottky limit for a barrier in absence of the interface states(given by the difference between the metal work function and the electron affinity of GaAs) and a probable pinned limit if barrier formation is dominated by interface states. Points labeled ST are contacts to UV grown, stoichiometric oxides. Points labeled GR are contacts to Ga-rich oxide surfaces.

limit. Again, this change is most extreme for the Ga-rich oxide surfaces, indicating a large change in interface state density for this case.

A GaAs surface with a Ga-rich oxide has been previously found by XPS to have less surface band bending than a surface with a stoichiometric oxide.[37] The reduced band bending at the surface was attributed to a reduction in the interface state density. It was suggested that this might occur when the stoichiometric oxide was annealed and Ga_2O_3 was formed in the reaction with the substrate. In our data, the interface state density appears to be reduced even for the stoichiometric oxide, but reduced further for the Ga-rich oxide. This may be due to the nonbonding, occupied orbital associated with the As_2O_3 molecule.[38] This bonding defect can act as a filled acceptor state on the surface. The reduction of the amount of As_2O_3 on the surface when a Ga-rich oxide is formed may be the reason for the larger variation of Schottky barrier heights observed for contacts to annealed oxides.

Our results are also in agreement with the recent unpinning of the GaAs surface using a photochemical process in flowing water. A possible explanation for the unpinning was a passivating Ga-oxide layer on the surface.[39] Our study, however, is the first to form Schottky contacts on a well characterized Ga-oxide rich surface where an increased variation in Schottky barrier height is demonstrated.

The similarity of behavior for metals reactive with the surface oxide layer, and metals inert to the surface oxide layer, indicates that chemical reactions involving the metal and the oxygen at the surface are not the dominant cause for the apparent reduction in interface states. It is not clear,

however, whether the increased Schottky barrier variation observed here is due to a change of surface states before metal deposition, or a change in the interface states formed during metal deposition. Oxygen at the surface may play a role in inhibiting alloy formation between Ga, As, and the metal overlayer.[40] Oxide compounds also give the semiconductor surface a more ionic character which would tend to decrease the density of the induced states when a metal is deposited.[41,42] This is consistent with the observed greater change in interface states for a Ga-oxide rich interface since Ga_2O_3 has a more ionic character than As_2O_3.

Hence, a much wider variation in Schottky barrier heights for contacts on GaAs (100) surfaces which had been oxidized using low intensity, deep UV illumination at room temperature was observed compared to contacts on clean GaAs surfaces. This has been interpreted as resulting from a change, most likely a reduction or spreading, of interface states in the metal-GaAs contact, since the Schottky barrier which results for metals deposited on the surfaces with oxides varies more strongly with the work function of the metal than Schottky barriers on clean GaAs surface. This change in interface states is especially pronounced for a stoichiometric oxide which has been annealed to form a Ga-rich oxide surface.

An investigation of the bulk traps in these samples was performed using deep level transient spectroscopy (DLTS). DLTS is one of the most useful techniques for investigation of bulk traps in semiconductor material. It provides a direct probe to evaluate the activation energy, concentration, and cross section of the traps. In order to make a DLTS measurement, a p-n

junction or a Schottky barrier is required.[43] In the Schottky barrier case, the DLTS signal is primarily from the trap states near the depletion layer edge away from the metal-semiconductor contact. Thus, the variation of Schottky barrier at the contact should not contribute to the DLTS signal. However, when we conducted a systematic DLTS measurement of the EL2 trap in GaAs using Schottky contacts wth barrier heights ranging from 0.54 to 0.93 eV, achieved by modifying the GaAs surface with an ultraviolet-light-enhanced oxide prior to metal deposition, the interpretation of the data was not so straightforward. It was found that for barrier heights between 0.62 and 0.83 eV, the DLTS signal saturates for barrier heights higher than 0.83 eV and disappears when barrier heights are below 0.62 eV. A calculation of the quasi-Fermi level under reverse bias was made to show that all three results can be interpreted by the variation of the quasi-Fermi level due to the barrier height change. The effect of Schottky barrier height on the deep trap signal must be taken into consideration in DLTS measurements, especially for low barrier height samples. The results of this study indicated that the trap may still exist in the material, even though it is not observed in some cases by DLTS. The DLTS was performed using a Boonton 72B capcitance meter and a dual channel boxcar averager with the rate window set at $200s^{-1}$. All measurements were made using a 2 V pulse of width 0.1 ms and a 2 V reverse bias supply. The peak of the EL2 spectrum occurred near 400 K and the activation energy of EL2 was found to be 0.83 eV below the conduction band. Figure 23 shows three typical signal curves. Curve (a) has the largest signal peak taken from Cu on a clean sample with a barrier height of 0.88 eV. Curve

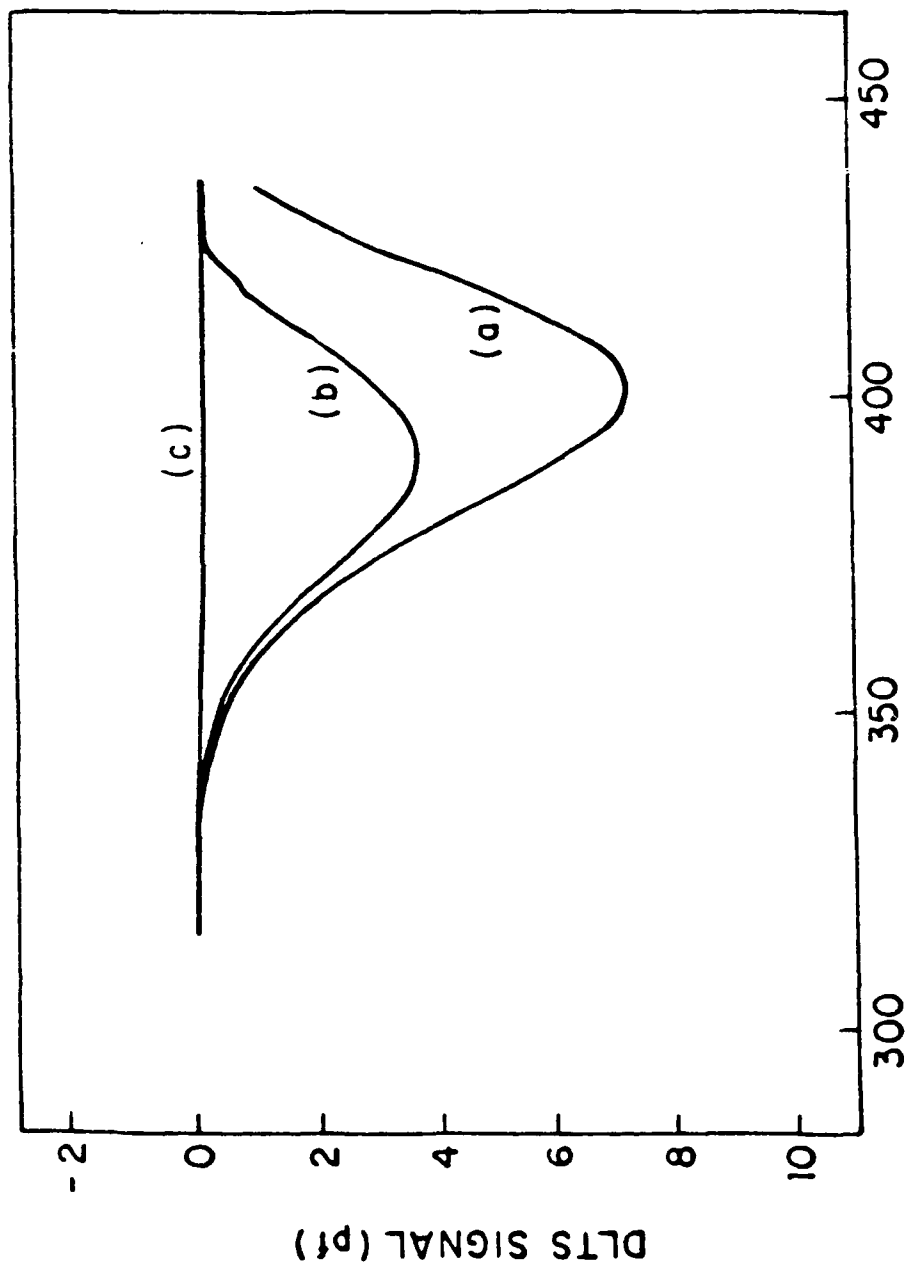


Figure 23. DLTS spectra of the EL2 trap in GaAs measured from (a) a clean Cu Schottky contact, (b) a clean Cr Schottky contact, and (c) a ST Cr sample with -2 V reverse bias, 2V/0.1 ms filling pulse and a rate window of 200 s^{-1}.

(b) is measured from Cr on a clean sample with a 0.73-eV barrier height. The peak height in this case is only half the magnitude of curve (a). For Cr on a stoichiometric oxide sample with a 0.62-eV barrier height, shown in curve (c), no signal is detected.

The measurement of other samples showed the same behavior and the data were reproduced many times. DLTS was performed on all of the samples listed in Table 3. The results are summarized in Fig. 24. There are basically three regions described as follows: (a) Saturation region: the signal reaches its maximum for barrier heights higher than 0.83 eV; (b) Transition region: the signal decreases as the barrier height decreases from 0.83 to 0.62eV; and (c) Disappearance region: the signal is not observed for barrier heights lower than 0.62eV.

In order to understand the characteristics of the EL2 signal in the three regions mentioned above, the position of the quasi-Fermi level in the depletion region under reverse bias was examined. The model for the quasi-Fermi energy calculation is based on the theory of carrier drift and diffusion through the depletion region.[44,45] For an n-type Schottky contact, the current density at a given bias voltage can be written as[44]

$$J = \frac{kT\mu N_c \{ exp[-F(w)/kT] - exp[-F(0)/kT] \}}{\int_0^w exp[-q\phi(x)/kT] dx}, \qquad (31)$$

where μ is the electron mobility, N_c is the effective density of states in the conduction band and kT is the thermal energy. F(O) and F(w) are the quasi-Fermi energies at the metal semiconductor interface and at the edge of the

Table 3. Barrier height ϕ_b on GaAs sample*

Samples	1	2	3	4	5	6	7	8	9	10	11	12
Metals	Cr			Ti			Cu			Pd		Ag
	CL	ST	GR	CL	ST	GR	CL	ST	GR	ST	GR	CL
$q\phi_b$(eV)	0.73	0.62	0.54	0.78	0.65	0.63	0.88	0.84	0.77	0.92	0.93	0.75

*CL, ST, and GR are explained in the text.

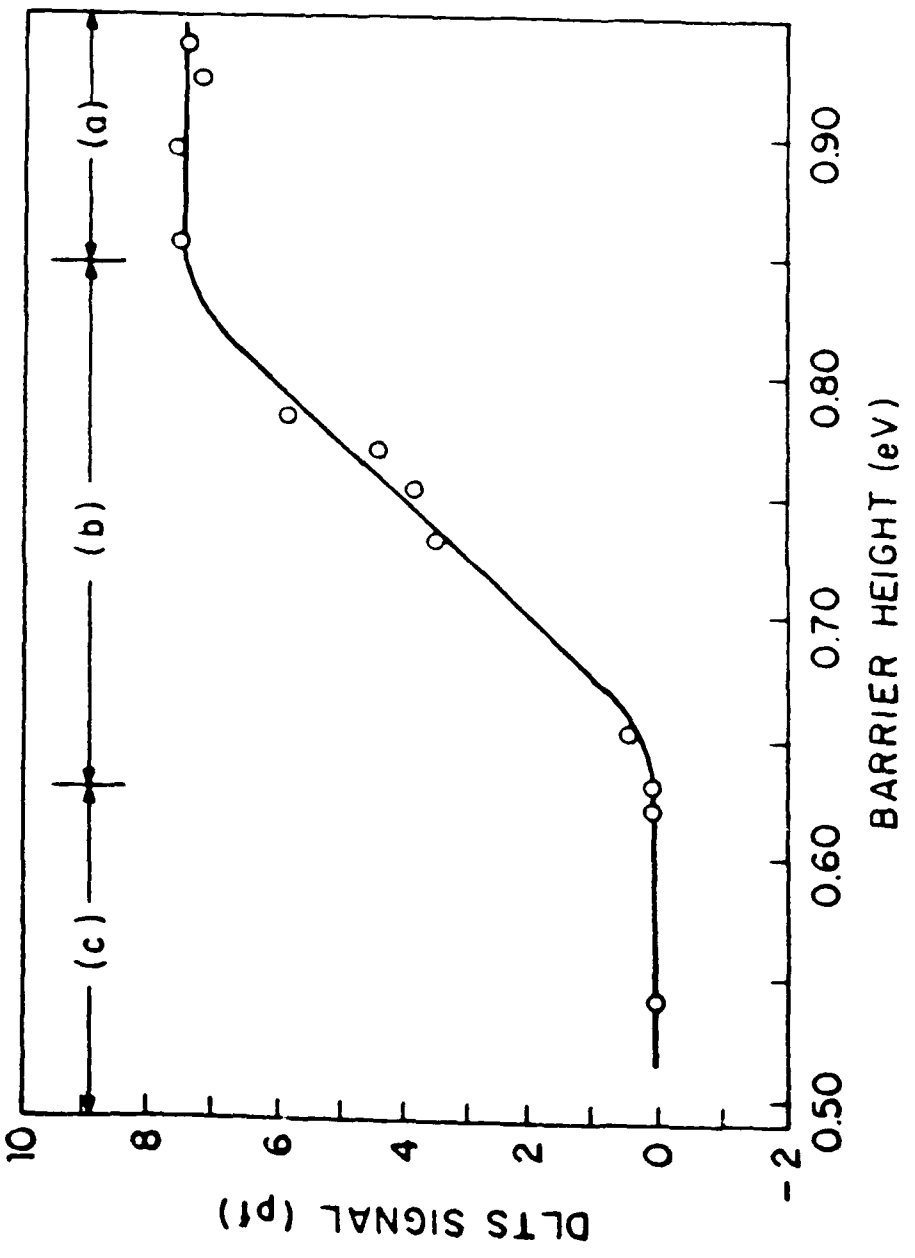


Figure 24. The peak intensity of the DLTS signal of EL2 vs. the Schottky barrier height.

depletion layer, respectively. For simplicity, the tunneling current and the image charge effect are neglected. The electric potential $\phi(x)$ in the depletion region is given by

$$\phi(x) = (qN_d/2\varepsilon)(2Wx - x^2) - \phi_b, \qquad (32)$$

where N_d and ε are the doping concentration and the permittivity of the semiconductor, ϕ_b is the barrier height, and W is the depletion layer width determined by $W = [2\varepsilon(\phi_b\text{-}V\text{-}kT/q)/qN_d]^{1/2}$ for a bias voltage V.

Using Eq.(32), the integral in Eq.(31) can be evaluated as

$$\int_0^{\infty} exp\left(\frac{-q\phi(x)}{kT}\right) dx = exp\left(\frac{q\phi_b}{kT}\right) LD(W/L), \qquad (33)$$

where $L = (2\varepsilon kT/N_d q^2)^{1/2}$ and D(W/L) is the Dawson function[46] defined as

$$D(W/L) = exp(-W^2/L^2) \int_0^{W/L} exp(y^2)\, dy. \qquad (34)$$

Experimental data for the barrier height, ϕ_b, and the reverse current density, J, are applied to calculate the quasi-Fermi level in the depletion region. Since the EL2 signal peak occurs near 400 K, as mentioned earlier, the reverse current at this temperature was measured. Figure 25 shows a plot of experimental results of reverse current density at 400 K versus the barrier height. It can be seen that as the barrier height decreases from 0.93 to 0.54eV, the reverse current increases by more than three orders of magnitude.

The barrier heights at 400 K were also measured, so as to match the condition of the DLTS measurements. It was found that the I-V characteristics were no longer linear and ideality factors were larger than 1.1 for low barrier height diodes ($\phi_b < 0.75$ eV). Thus, the determination of the

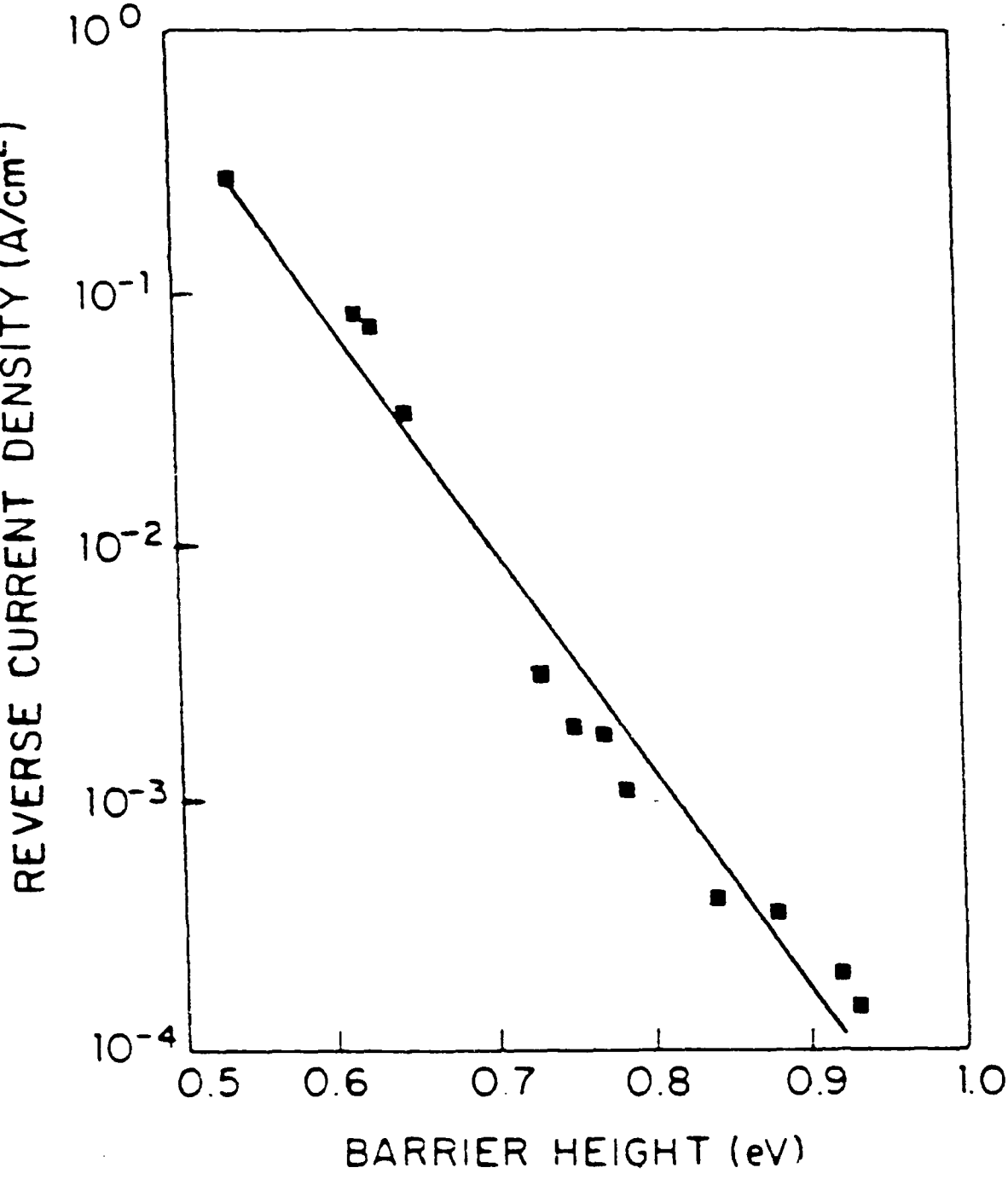


Figure 25. the reverse current density measured at 400 K for the various Schottky barriers.

barrier heights for these samples becomes unreliable. However, it is commonly assumed that the barrier height is essentially temperature independent over a moderate range of temperature.[47] Therefore, the room temperature values of the barrier height in Table 3 are used in this study.

Results of the quasi-Fermi energy calculation from Eq.(31) for three typical samples with barrier heights of 0.88, 0.73, and 0.62 eV are plotted in Fig. 26. The reverse bias is set at 2 V, as was applied in the DLTS measurements. Under this reverse bias, a length D is defined as the distance from the metal-semiconductor interface to the point where the trap level crosses the quasi-Fermi level. Inside this region, electrons could be trapped in the EL2 level during the filling pulse and be remitted to the conduction band after the pulse and hence contribute to the DLTS spectra. For comparison, Fig. 26(d) gives the quasi-Fermi level during the pulse, which corresponds to zero bias on the Schottky diode. The result of the quasi-Fermi level, F, in this case, is flat and lines up with the metal Fermi level F_m. The EL2 level E_t is basically occupied in the depletion region.

The probability of electron occupancy for a trap state is given by

$$p(E_t) = \frac{c_n n + c_p p_1}{c_n n + c_n n_1 + c_p p + c_p p_1} \qquad (35)$$

where $c_n(c_p)$ is the capture cross section for electrons (hole) multiplied by the thermal velocity, n(p) is the mobile electron (hole) density and $n_1(p_1)$ would be the concentration of electrons (holes) if the quasi-Fermi level coincided with the trap level. When the state can be considered to be in equilibrium with the conduction band this reduces to

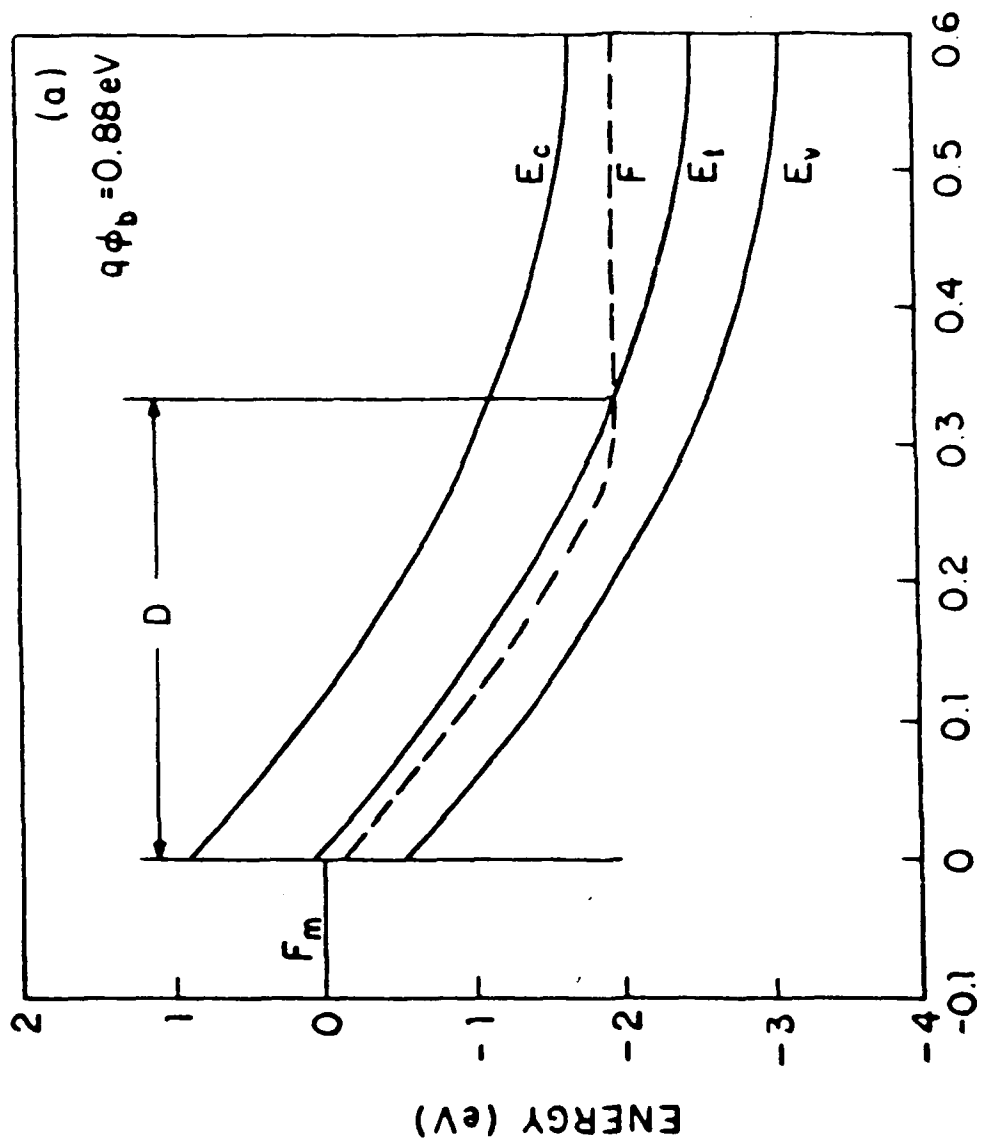
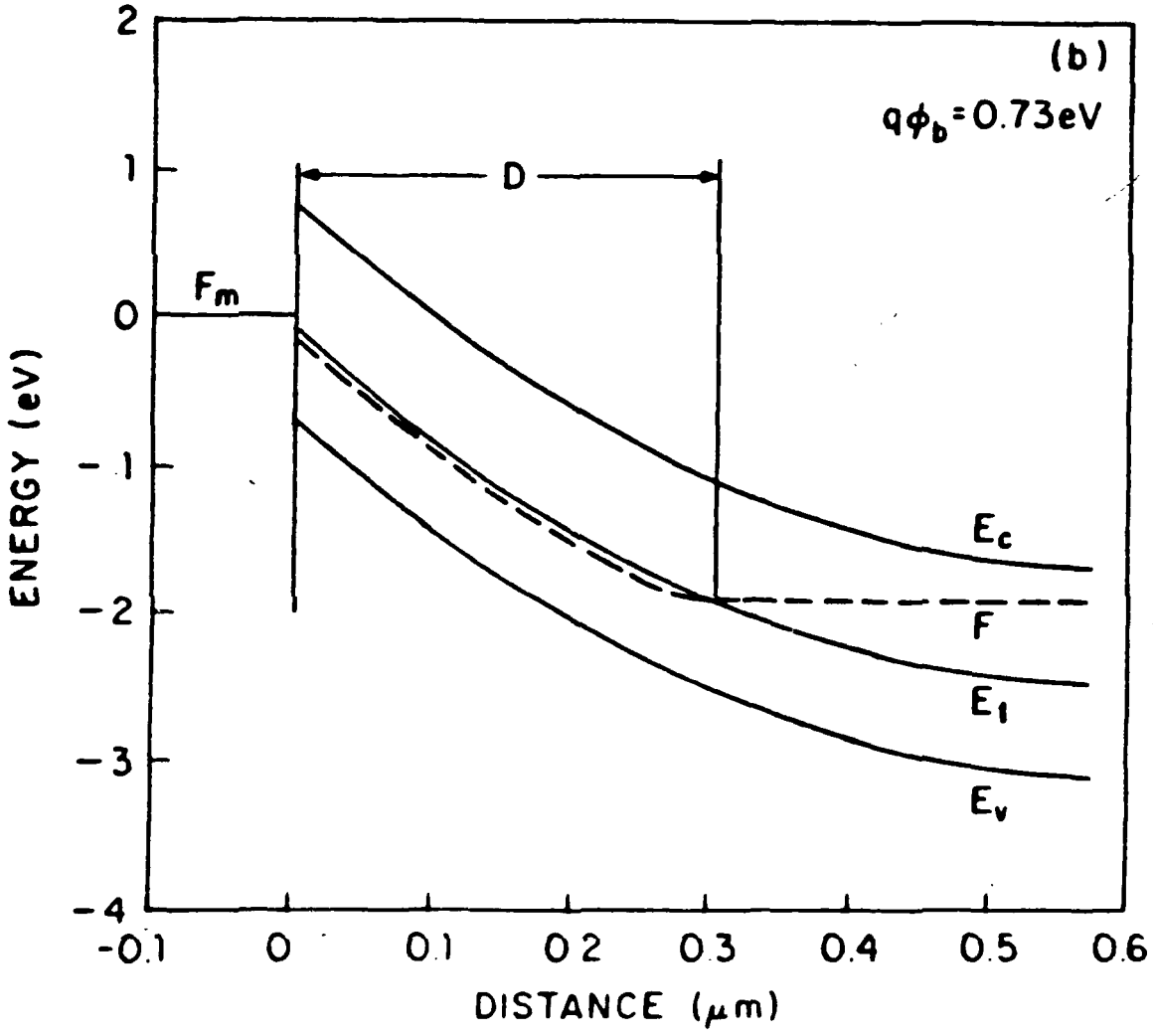
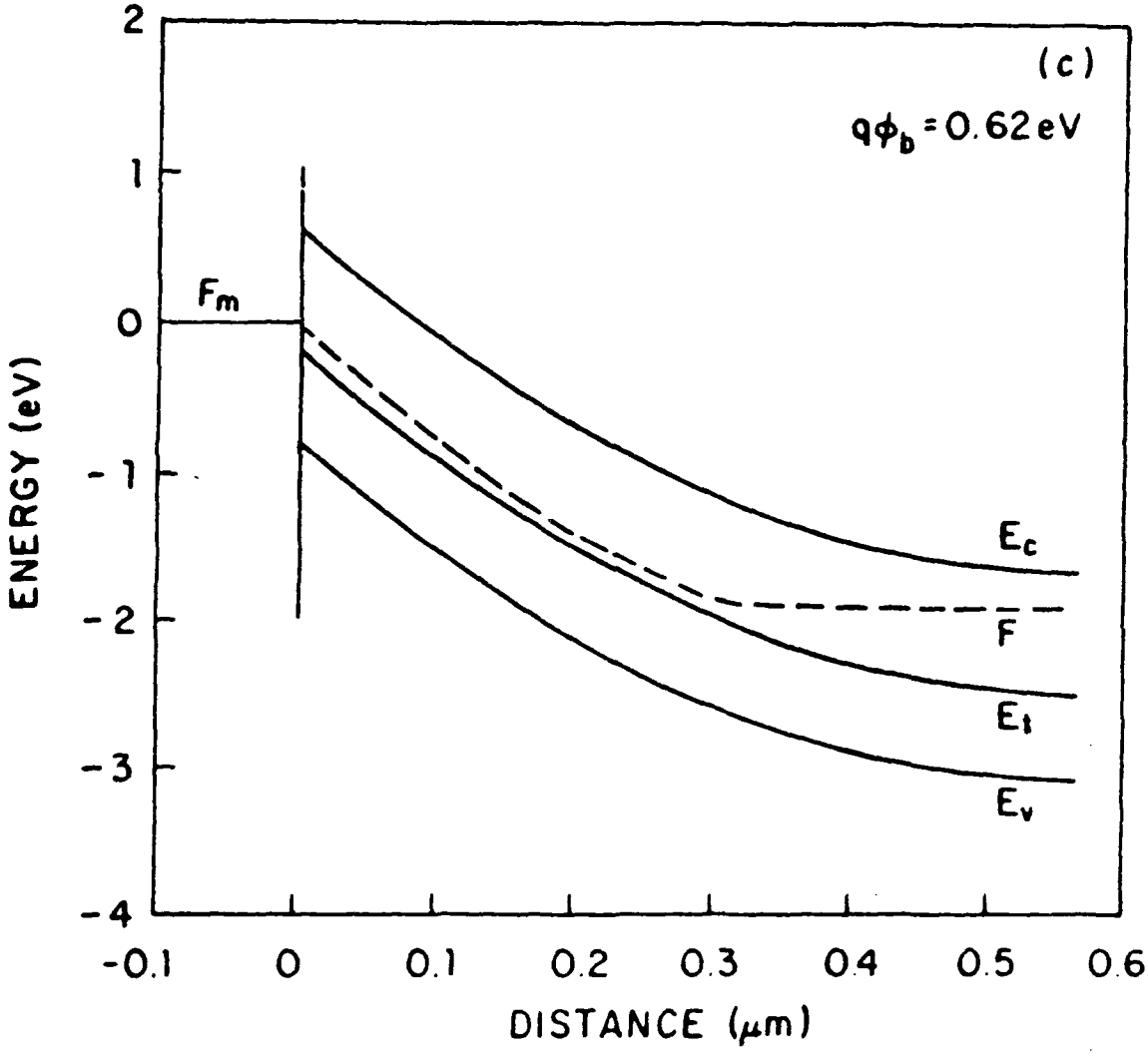
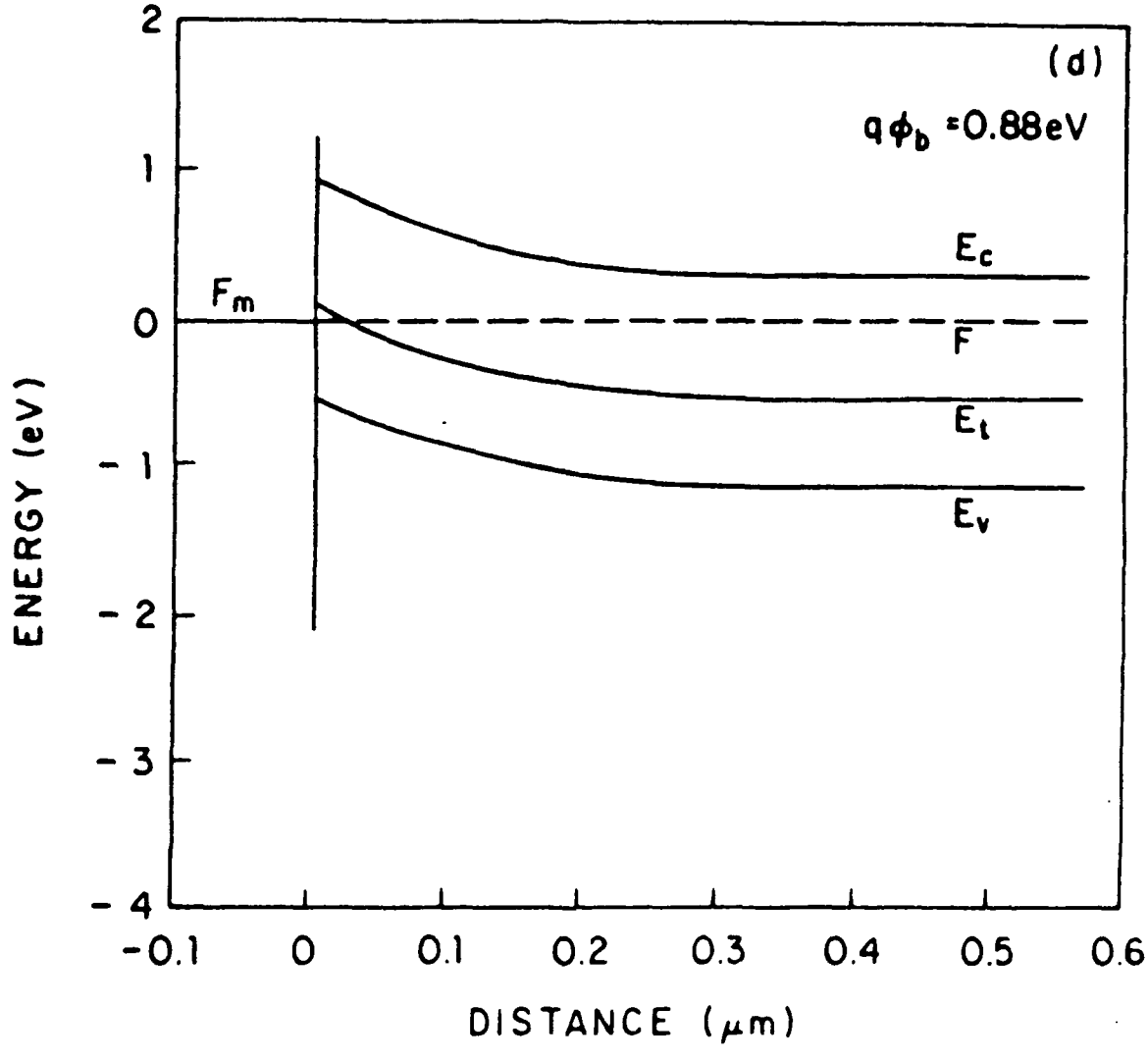


Figure 26. The quasi-Fermi level and band diagram under 2 V reverse bias for (a) a clean Cu sample (b) a clean Cr sample (c) a ST Cr sample and (d) the Fermi level and band diagram of (a) under zero bias (pulse filling process)


(b)
$q\phi_b$=0.73eV
D
F_m
E_c
F
E_i
E_v
ENERGY (eV)
DISTANCE (μm)
2
1
0
-1
-2
-3
-4
-0.1
0
0.1
0.2
0.3
0.4
0.5
0.6


(c)
$q\phi_b = 0.62\,eV$
F_m
E_c
F
E_t
E_v
ENERGY (eV)
DISTANCE (μm)
2
1
0
-1
-2
-3
-4
-0.1
0
0.1
0.2
0.3
0.4
0.5
0.6


(d)
$q\phi_b$ =0.88eV
E_c
F_m
F
E_t
E_v
ENERGY (eV)
2
1
0
-1
-2
-3
-4
-0.1
0
0.1
0.2
0.3
0.4
0.5
0.6
DISTANCE (μm)

$$P(E_t) = 1/\{1 + exp[(E_t - F)/kT]\}, \qquad (36)$$

where E_t and F are the trap state energy and the Fermi level. If the trap level is far below the Fermi level (E_t - F < - 3kT), $P(E_t) \approx 1$, and almost all trap states are occupied. If the trap level is far above the Fermi level (E_t - F > 3kT), $P(E_t) \approx (E_t - F)/kT] \approx 0$, and most of the trap states are empty.

In the high barrier height case of Fig. 26(a), the quasi-Fermi level under reverse bias is far below the EL2 level inside the length D. Et - F ≈ 0.2 eV ≈ 6 kT, so that the probability of occupancy for EL2 states is very low. When a filling pulse is applied during the DLTS measurements, these states can trap and emit electrons to produce a maximum signal. At the low barrier height, Fig. 26(c), the quasi-Fermi level is above the EL2 level (Et - F ≤ - 4kT) through the whole depletion region and the length D shrinks to zero. All EL2 states are basically occupied, both under the reverse bias and during the filling pulse process. In this situation, the EL2 states are electrically inactive so that no signal can be observed. For barrier heights between 0.62 and 0.83 eV, Fig. 26(b), the quasi-Fermi level is very close to the EL2 level in length D. In other words, - 3kT < E_t - F < 3kT and the EL2 states are partially empty. Those empty states can participate in the trapping and emitting process to yield an intermediate signal. As the barrier height decreases form 0.83 to 0.62 eV, the quasi-Fermi level will move up and cross the EL2 level. This results in fewer empty states inside the depletion region. Hence, the DLTS signal becomes proportionally smaller.

The signal intensity observed in the DLTS thus depends on the number of active trap states when the bias is switched, rather than the trap density

itself. For the EL2 midgap level, the traps are almost fully occupied at zero bias. Therefore, the signal intensity in the DLTS reflects the number of empty states under the reverse bias. For the barrier height greater than 0.83 eV, all of the EL2 states are empty in the depletion region. The DLTS signal reaches its maximum and saturates. As the barrier height decreases, the occupancy of the EL2 state increases. The intensity of the DLTS signal attenuates accordingly. At very low barrier height (ϕ_b < 0.62 eV), the EL2 states are constantly far below the quasi-Fermi level. They become inactive in the DLTS measurements. As a result, the EL2 signal disappears. Similar analysis may apply to other traps with an activation energy near the midgap. The three cases of DLTS signal variation for such traps could be obtained if an appropriate range of Schottky barrier height is available.

Other effects on the DLTS signal of EL2 were also investigated. All DLTS measurements and quasi-Fermi level calculations were carried out under the same 2 V reverse bias condition which yields a maximum electric field of 8 x 10^4 V/cm. This field is too low to result in an enhanced emission rate for the EL2 level observed at high fields (> 3 x 10^5 V/cm).[48,49] For samples with barrier height below 0.62 eV, the reverse-bias pulsed deep-level transient spectroscopy (RDLTS)[48] has been used to check the field effect. Even for devices which have the largest reverse current, the EL2 signal is still not observed for a field as high as 4.5 x 10^5 V/cm (reverse bias of 15 V). It can be concluded that the variation and the disappearance of the EL2 signal in this study are mainly due to the variation of the quasi-Fermi level in the

depletion layer. This variation of the quasi-Fermi level is caused by the different barrier height of the Schottky contacts.

The effect of Schottky barrier height on trap signal has to be given strong attention in the DLTS measurement. For low barrier height samples, the disappearance of the trap signal may be misinterpreted as a property of the measured material. Therefore, to obtain the actual trap density for midgap traps, contacts with high Schottky barriers are preferred for DLTS measurement.

Chapter 3 - Interpretation of Anomalous Reverse Bias Capacitance Measurements

The value of the Schottky barrier height is established using three different techniques - current voltage, internal photoemission, and reverse bias capacitance voltage measurement. For silicon diode these three methods give results which usually agree to within 50 meV. However for GaAs devices, we have found that the capacitance measurements cannot easily be interpreted in terms of barrier height and doping density. The devices described in the last chapter were subjected to reverse C-V analysis and the $1/C^2$ vs. V curves were found to have nonlinear regimes and intercepts much larger than the built in potential. In this chapter we will discuss these measurements, eliminate deep bulk traps as a possible cause and suggest a model to explain the results based on interface states.

For a semiconductor with a constant doping density the reverse biased capacitance is given by

$$C = \sqrt{\frac{q \varepsilon_s N_D}{2} \frac{1}{(V_{bi} + V)}} \qquad (33)$$

where ε_S is the dielectric constant of the semiconductor, N_D is the doping density, V the applied reverse bias and V_{bi} the built in potential. A plot of $1/C^2$ vs. V then has a slope proportional to $1/N_D$ and an intercept on the voltage axis giving V_{bi}. Deviations from this ideal behavior can be due to a nonuniform doping density, the presence of bulk traps or interface charge.

We have determined the reverse C-V characteristics for the diodes discussed in Chapter 2. The measurements were performed using a standard Boonton capacitance meter with a 15 mV small signal at 1 MHz. Devices with a clean GaAs surface, a stoichiometric oxide, and a Ga rich oxide were analyzed for T_i, Pd, Cr, and Ni metallization. Certain salient features of the data were present independent of the specific metal. In all cases the high voltage portion of the $1/C^2$ vs V curve was linear with a voltage intercept anywhere from .6eV to 1.8eV greater than the built in potential as measured by internal photoemission or I-V techniques. The discrepancy was always greatest for the Ga rich oxides. The slope of this linear region was within a factor of three of the ideal value given by the doping density measured using a four point probe. Furthermore the deviation from linearity over the whole reverse bias voltage range became more prominent as we progressed from the clean surface to the Ga rich oxide. A typical set of results for Pd/nGaAs with three different surface preparations is shown in Fig. 27.

We can immediately conclude that a nonuniform doping density cannot be responsible for the observed results. Such doping would result in a $1/C^2$ vs V curve which has no linear region. As can be seen from Fig. 27 the higher reverse bias portion for all the different interface structures is quite linear. If the nonuniform doping density simply occured near the surface as a result of the metal deposition process than the high voltage regime would be linear with a slope giving the nominal doping density. This is indeed the case. However, the voltage axis intercept of this linear asymptote would give the

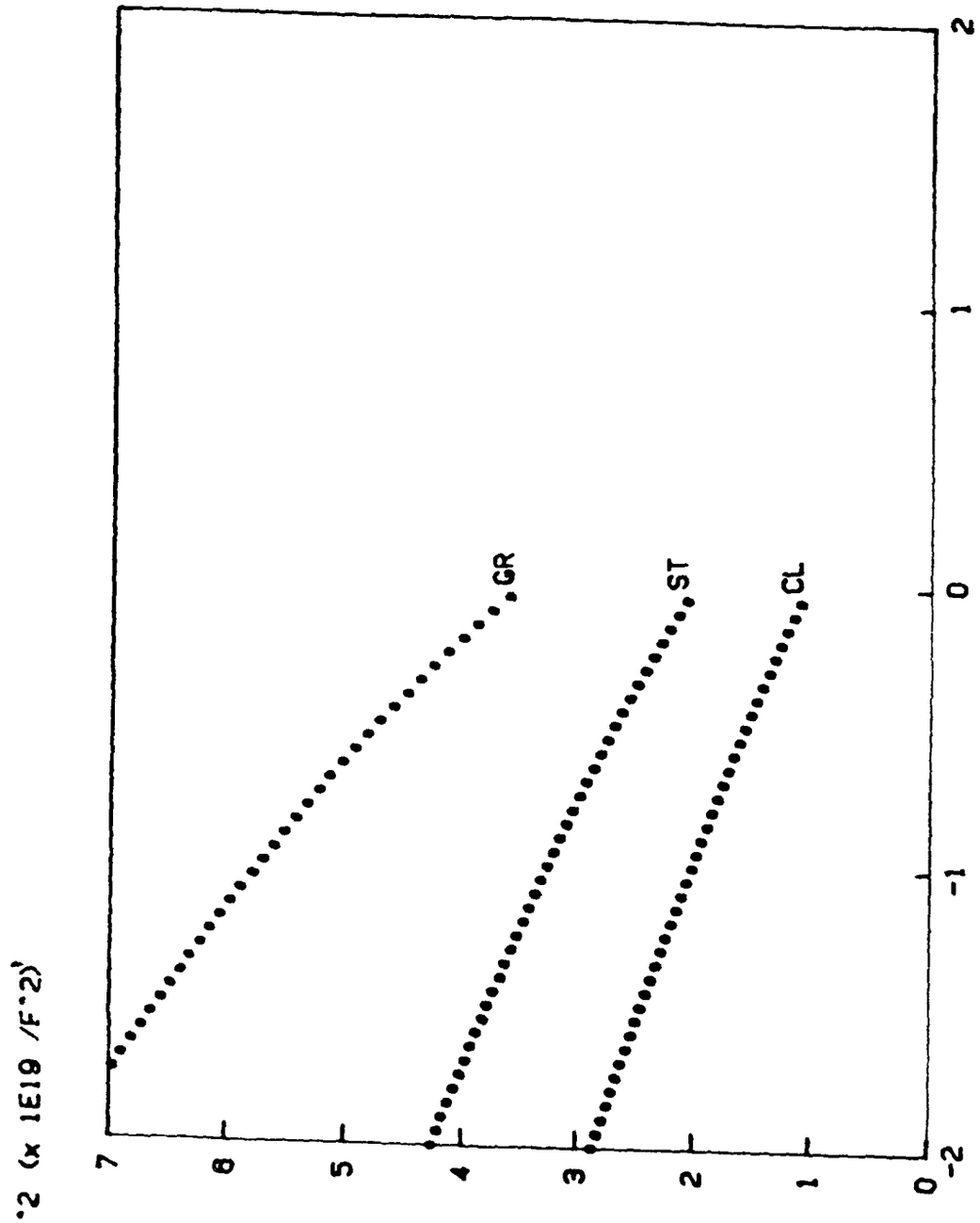


Figure 27. Reverse bias $1/C^2$ vs. V curves for Pd/n-GaAs diodes with a clean surface, a stoichiometric oxide, and a Ga rich oxide.

proper built in potential and not an intercept which differs from the IV and photoemission measurement by as much as 1.8 eV.

The effect of deep traps is not as obvious and was analyzed as follows. Deep level transient spectroscopy measurements were made to determine the concentrations and energies of the various trap states. In a typical sample significant density of EL2, EL3, EL5, EL6, and EL8 centers were discovered. The concentration of these states in terms of the doping denisty N_d was $.08N_d$, $.10N_d$, $.04N_d$, $.12N_d$, and $0.2N_d$ respectively as shown in Fig. 28. We assume that these states cannot respond to the high frequency small signal so that the measured capacitance is still given by

$$C = \frac{e_s A}{W_d} \tag{38}$$

However, the depletion layer width, W_d, depends now on both the doping density and the occupancy of these states. At a given reverse bias voltage the states are occupied when they are below the electron quasi-Fermi level, E_f, and unoccupied above. It is further assumed that at the end of the depletion region all the deep levels lie below E_f and contribute no net charge. By measuring the reverse bias current we determine the relative distance between E_f and the conduction band edge, E_c (and hence the trap levels E_{tt}) in this region using

$$Jr = q\,\mu n(dE_f/dx) = f(E_c, E_f) \tag{39}$$

and Poisson's equation

$$d^2E_c/dx^2 = +\ \rho/e_s \tag{40}$$

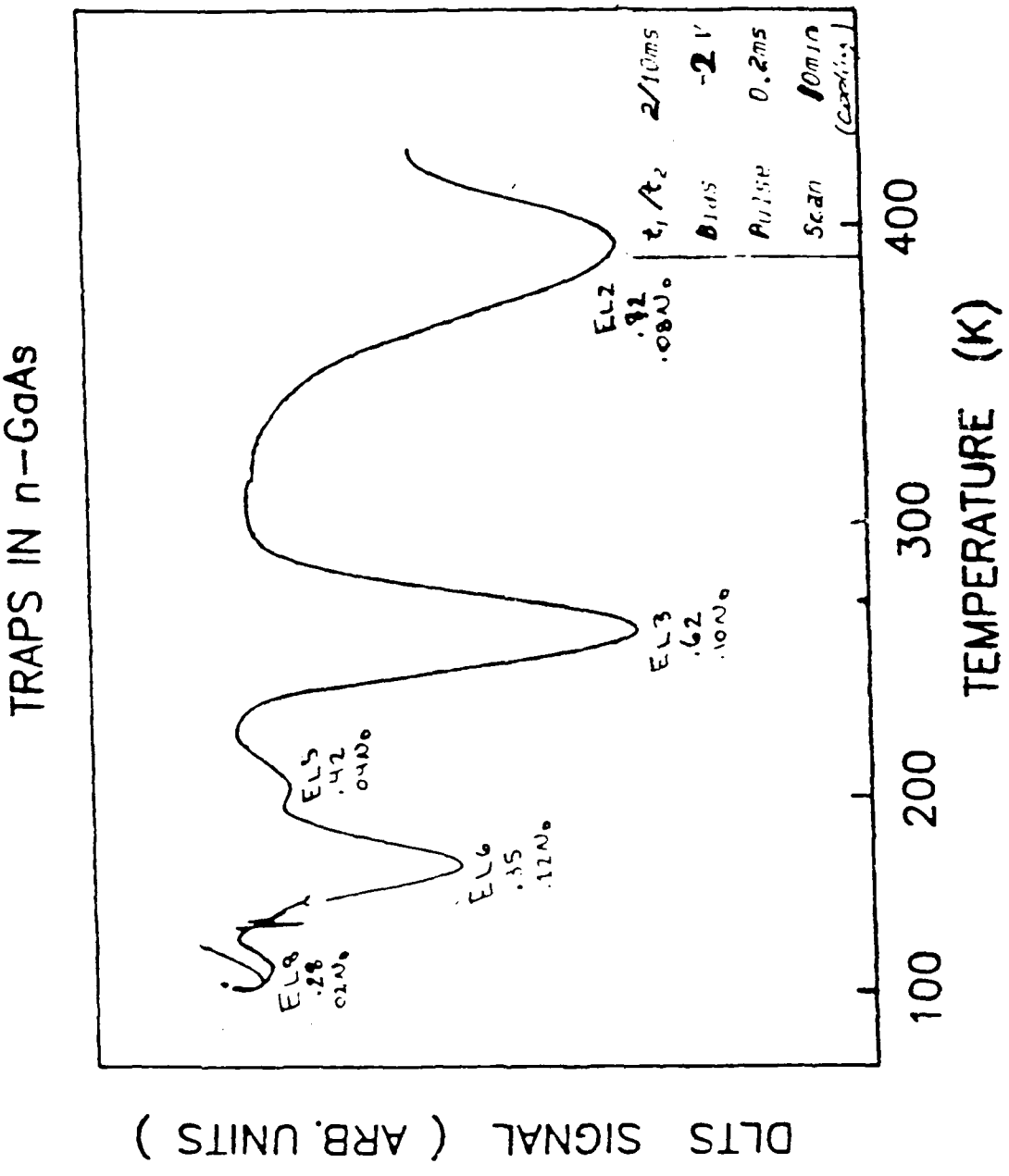


Figure 4d. DLTS spectrum for traps in n-GaAs.

Proceeding from the edge of the depletion region towards the interface we find the position x_1 where E_f crosses the shallowest trap level. For $x < x_1$ we must take into account charge cotnributed by this trap in solving Poisson's equaiton and determining E_f and the crossover point x_2. In this manner the distance from the interface, x_i, where i^{th} trap crosses the quasi Fermi level can be determined for any given reverse bias voltage and for each of the specified levels.

The charge contributed to the depletion region by the various trap levels and hence the shape of the conduction band edge depends on the reverse bias voltage. The capacitance is then derived as

$$qN_d\varepsilon_s/2(1/C^2) = \left(V_a + q/\varepsilon_s \sum \int_{x_t}^{0} \int_{x_t}^{x'} N_T^t dx'' dx'\right) + V_{bi} \qquad (41)$$

where the second term on the right is due to the deep levels of concentration N_T^t which cross the Fermi level at x_t under reverse bias V_a. Using the values of x_t determined as described previously at each reverse bias we plot

$1/C^2$ vs $V_a + q/\varepsilon_s \sum \int_{x_t}^{0} \int_{x_t}^{x'} N_T^t dx'' dx'$ to yield the intercept V_{bi}. This reconstructed $1/C^2$ curve is shown in Fig. 29 where the original data points are represented by the "o"'s and the "+"'s take into account the traps. As easily seen, the shift due to the deep levels is not large enough to explain the anomalous intercept. Another explanation needs to be developed in order to understand these curves.

The effect of interface states and an interfacial layer on the reverse bias diode capacitance had been introduced by Cowley[50] and reviewed by

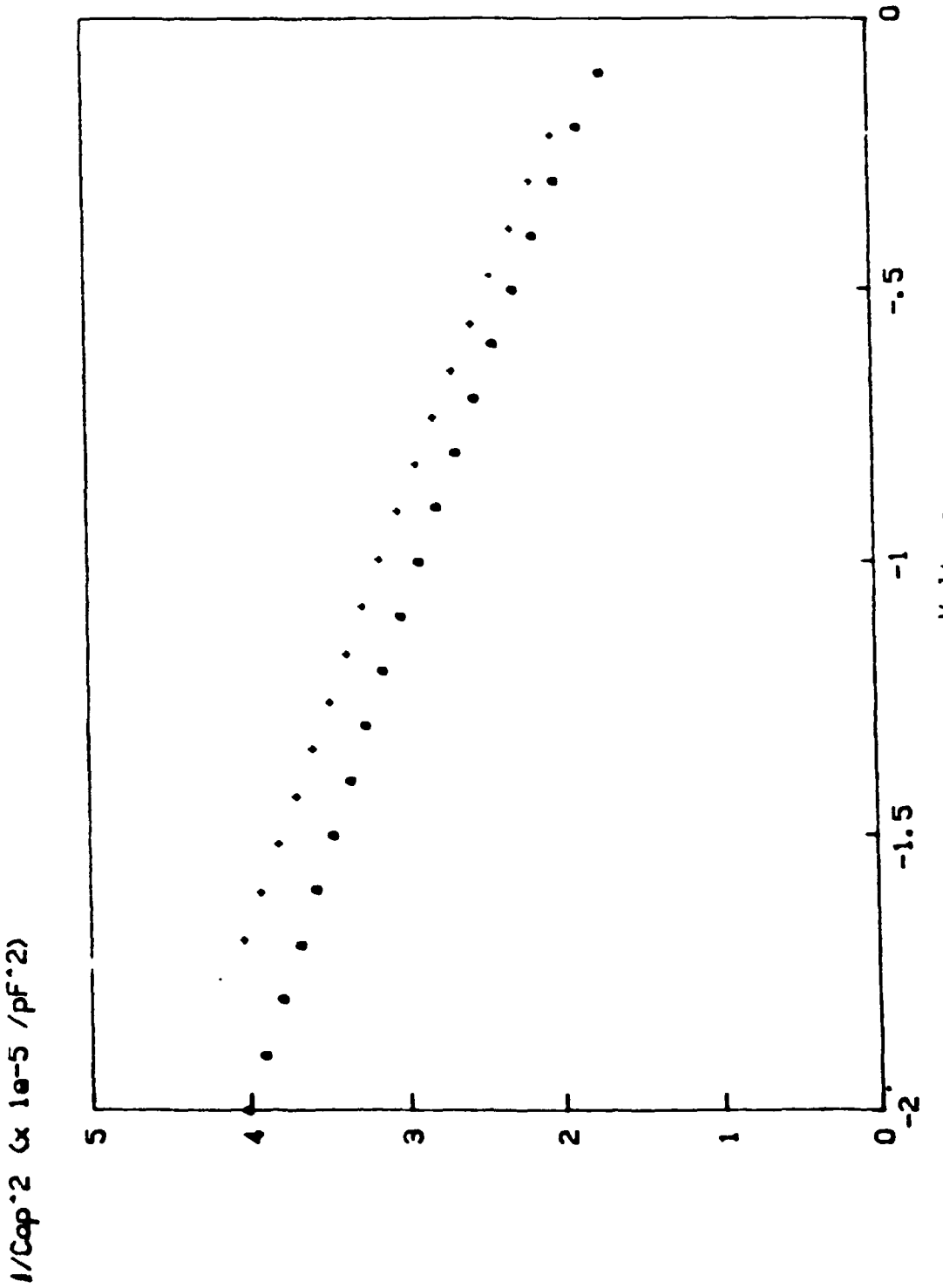


Figure 29. Reconstructed $1/C^2$ vs. V curve for a Ni/n-GaAs diode with a clean surface taking into account the effect of bulk level traps in the GaAs.

Fonash [51] More recently Callegari et al.[52] encountered high intercepts on GaAs with 2.5 nm of oxide and postulated a constant density of states throughout the bandgap to account for the data. The intercepts however were not quite as large as the ones we have noted nor were there extensive non linear regimes. In our case a constant density of states is not applicable because the result will always be a perfectly linear $1/C^2$ vs V curve. Our model builds on these previous theories by removing the necessity of a constant density of traps and replacing it wiht one or two finite bands of states of independent width ($E_{2i} - E_{1i}$) and denisty (N_{Si}) in the bandgap. These states cannot respond at the small signal frequency but change their occupancy with the DC bias. For each band a fraction (β_i) of the total density is assumed to be in equilibrium with the metal and has an occupancy given by the relative position of the metal Fermi level and the trap energy at the interface. The remaining states have statistics based on the semiconductor Fermi level in the bulk. A portion of the applied bias is dropped across the interfacial layer with the remainder taken up by the semiconductor depletion region. The total applied voltage V can be written as

$$V = (V_{bi} - V_{bi0}) + (\Delta - \Delta_0) \qquad (42)$$

where V_{bi} (Δ_0) is the built in voltage across the depletion region (interface layer) and $V_b(\Delta)$ is the total band bending in the semiconductor (interface region). If the net change in charge from equilibrium in the the interface is given by Qs, Eq.(42) can be written as

$$V = V_{bi} - V_{bi0} + V_1^{1/2} - \left(V_b^{1/2} - V_{b0}^{1/2}\right) + \frac{\delta}{\varepsilon_i} Q \qquad (43)$$

where δ and ε_i are the width and dielectric constant of the interface layer.

We initially postulated a single band of states in the bandgap surrounding the equilibrium position of the Fermi level. At low voltage both the semiconductor and metal Fermi levels are moving through this band and hence the occupancy of the states in equilibrium with the metal and those in equilibrium with the semiconductor changes with bias. The resulting capacitance can be derived by solving for V_b using Eq.(43) and then deriving the capacitance as

$$C = \frac{dQ_{sc}}{dV} = \frac{dQ_{sc}}{dV_b}\frac{V_b}{dV} = \frac{\varepsilon_i}{\delta}\frac{V_1^{1/2}}{2} V_b^{-1/2}\left(\frac{1 + \frac{\delta}{\varepsilon_i} q\beta_1 N_{st}}{1 + \frac{V_1^{1/2}}{2} V_b^{-1/2} + \frac{\delta}{\varepsilon_i} q(1-\beta_1)N_{s1} + \frac{\delta}{\varepsilon_i} q\beta_1 N_{s1}} \right) \quad (44)$$

where Q_{sc} represents the semiconductor space charge and V_1 is given as

$$V_1 = 2 q \varepsilon_s N_D \left(\frac{\delta^2}{\varepsilon_i^2} \right) \quad (45)$$

At high bias both the metal and semiconductor Fermi levels have moved through the band at states and there is no change in interface charge with bias. In other words, the change from equilibrium of the charge stored at the interface is a constant Q independent of bias in this region. The resulting capacitance is then given as

$$C = \frac{\varepsilon_i}{\delta} \frac{V_1^{1/2}}{2} V_b^{-1/2}\left(\frac{1}{1 + \frac{V_1^{1/2}}{2} V_b^{-1/2}} \right) \quad (46)$$

The slope of the $1/C^2$ vs V curve is inversely proportional to the doping

density and the intercept can be derived as $V_1^{1/2} V_{bi}^{1/2} + V_2 + \frac{V_1}{4} - \frac{\delta}{\varepsilon_i} Q$ Hence the large intercepts seen in the experimental data can be explained in terms of negative charge stored in the interface states under high bias.

This model has been applied to the GaAs samples by finding the best asymptotes for the high and low voltage regimes. The slope and intercept of the low voltage asymptote is expressed in terms of a parameter U given as

$$U = \frac{1 + \frac{\delta}{\varepsilon_i} N_{s1}}{1 + \frac{\delta}{\varepsilon_i} \beta_1 N_{s1}} \qquad (47)$$

For the case of Pd on both stoichiometric and Ga rich oxides the results are shown in Figs. 30 and 31. As we proceed from the clean surface to Ga rich oxide, U decreases from 1 to 0.61. This results from either an increase in δ or a decrease in β_1. Furthermore the region of validity of the low field regime increases as we proceed from the clean surface to the Ga rich oxide. This could be interpreted as a spread out in the states or a decrease in the density of states around the metal Fermi level. Both explanations are consistent with the shift towards more dependency of the Schottky barrier on the metal work function for the Ga rich oxides.

Although this model can explain qualitative features of the data, quantitative matching cannot be made with reasonable values for the interface parameters. We are now developing a more general model which postulates two bands of states, one opposite the metal Fermi level and one either above or below it. Instead of only considering asymptotic cases where

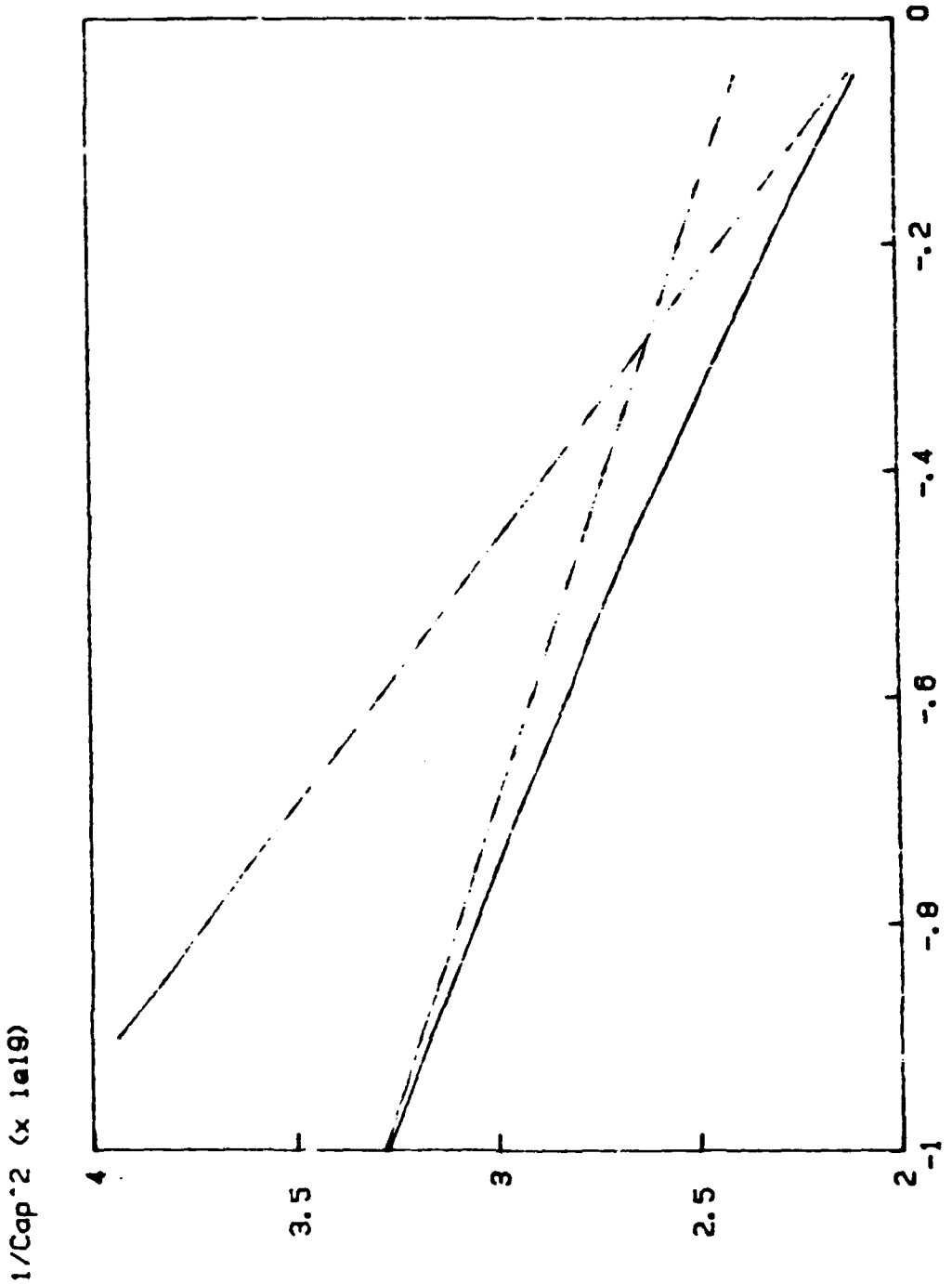


Figure 30. Asymptotic fit to the $1/C^2$ vs. V curve for a Pd/n-GaAs diode with a stoichiometric oxide using a single band of states which changes in the occupancy only at low reverse bias.

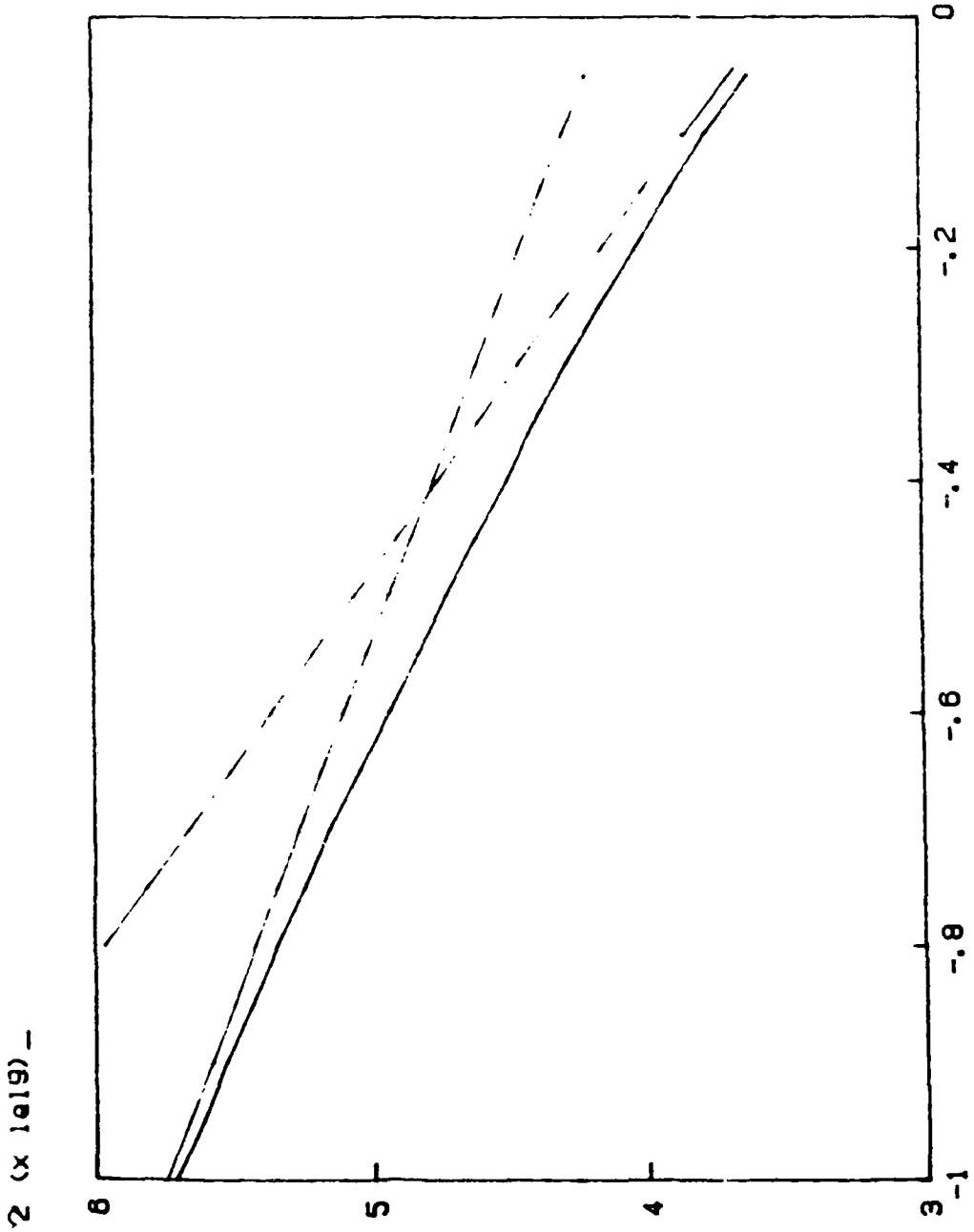


Figure 31. Asymptotic fit to the $1/C^2$ vs. V curve for a Pd/nGaAs diode with a gallium rich oxide using a single band of states which changes in occupancy only at low reverse bias.

both Fermi levels are either moving through a single band or are both outside the band as was done in the original formulation, six distinct possibilities now exist. For example, if one band lies opposite the equilibrium metal Fermi level and the other is below it, then at a given reverse bias, the metal Fermi level can either be inside or above the upper band. The semiconductor Fermi level can then lie in the same band, between the two bands or in the lower band. For all of these cases the band bending V_b can be determined using Eq.(43) where Q is still the change in interface state charge from equilibrium but must be carefully evaluated to include contributions from both bands and Fermi level shifts. The capacitance is then be derived at each value of applied voltage as

$$C = \frac{\varepsilon_i}{\delta} \frac{V_1^{1/2}}{2} V_b^{-1/2} \left(\frac{1 + \frac{\delta}{\varepsilon_i} \beta_m N_{sm}}{1 + \frac{V_1^{1/2}}{2} V_b^{-1/2} + \frac{\delta}{\varepsilon_i} q(1 - \beta_s) N_{ss} + \frac{\delta}{\varepsilon_i} \beta_m N_{sm}} \right) \quad (48)$$

where the subscript m designates the band in which the metal Fermi level lies and s represents the band being crossed by the semiconductor Fermi level. The gives a point by point evaluation of the capacitance when the position of the bands and density of the states are appropriately chosen.

Although we have derived all the necessary equations for these models, simulations have not yet been performed. However, it should be noted that this work is not in contradiction with any theoretical speculation on the Fermi level pinning in GaAs. Furthermore, the large intercepts would not be expected in silicon because of the much lower density of interface states (see

Chapter 1). Using $N_s = 10^{12}/cm^2/eV$ with a 10 A interface layer and a 1 eV wide band a first order approximation of the shift in intercept $\left(\frac{\delta}{\varepsilon_i} qN_{ss}\right)$ gives 10^{-2} eV. In GaAs on the other hand where Ns is expected to be close to $10^{14}/cm^2/eV$ the shift is on the order of 1 eV, similar to what we have recorded in our measurement.

We are now at a very interesting junction in our work in the sense that our capacitance measurements have come full circle. For Si with less interface states it is necessary to employ forward bias capacitance techniques while in GaAs the reverse bias capacitance is strongly effected by the states. We hope to receive appropriate funding to continue this work which we feel will explain the small range of Schottky barrier heights in GaAs and lead to more useful devices and circuits.

Conclusion

The studies described in this report have provided new insight into the formation and control of Schottky barrier diodes. The results can be considered as a springboard for future work which will lead to an in-depth understanding of the physical mechanisms governing the formation and degradation of metal semiconductor junctions. The most significant conclusions are as follows:

1) The interface state density for silicon Schottky diodes decreases upon annealing and formation of silicide and is in the $10^{12}/cm^2$ range.
2) The density of interface states can be correlated with the structural perfection of the junction.
3) A thin oxide at the GaAs surface results in a wide range of controllable Schottky barrier heights.
4) Deep level transient spectroscopy data for midgap traps is dependent on the device barrier height.
5) Anomalous reverse bias capacitance vs voltage data, including nonlinear $1/C^2$ vs V curves with high voltage intercepts, for GaAs diodes can be attributed to the high density of interface states.

The characterization techniques described need to be explored and further developed. For interface state densities less than $10^{12}/cm^2$ it is necessary to use forward bias capacitance spectroscopy to reveal the signature of the states. However, when the density of states is an order of magnitude greater, reverse bias capacitance techniques can be used if interpreted correctly. These two

methods provide a wealth of previously untapped information crucial to understanding the metal semiconductor contact.

FOOTNOTES

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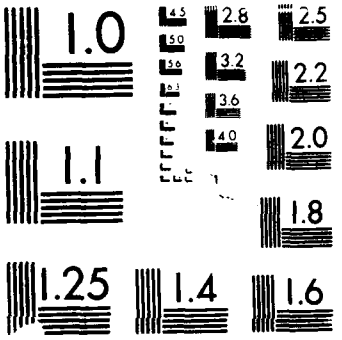
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6.3

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RADC plans and executes research, development, test and selected acquisition programs in support of Command, Control, Communications and Intelligence (C^3I) activities. Technical and engineering support within areas of competence is provided to ESD Program Offices (POs) and other ESD elements to perform effective acquisition of C^3I systems. The areas of technical competence include communications, command and control, battle management, information processing, surveillance sensors, intelligence data collection and handling, solid state sciences, electromagnetics, and propagation, and electronic, maintainability, and compatibility.

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